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DESIGN OF CIRCUITS FOR THE PATTERN ARTICULATION UNIT

by

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1.0 INTRODUCTION

The Pattern Articulation Unit (PAU) which has been described elsewhere contains a central core of 1024 identical processing modules called 'stalactites' arranged in a two-dimensional array with only local connectivity. Two possible complete circuit realizations of the stalactite will be described here. These realizations are not independent and other combinations of the component circuits are quite possible, though each as described follows a somewhat different design philosophy. Stalactites of either design will contain about 50 transistors, 500 diodes, 250 resistors, and 50 capacitors.

1.1 STALACTITE ORGANIZATION

A schematic representation of the stalactite organization as adapted from File No. 463 is shown in Figure 1. Four salient features may be observed. These exist:

1. Eight input lines from which data from eight nearest-neighboring stalactites may be received.
2. An output capable of returning signals to these eight neighbors.
3. An input and output associated with register M, and used in communication to other devices, the Transfer Memory, and Pyramidal Readout.
4. A logic assembly controlled by 40 externally-actuated control lines.

The majority of the control lines are common to all 1024 stalactites and are operated at the same time for each. Thus identical commands are given to occur in all modules at once. However, the process which results in each may be different and depends in general on the behavior of the neighboring [illegible] parallel processors.

Report No. 22. "The Design of a Pattern Recognition Digital Computer," by B. McCormick.

File No. 463. "The Design of a Pattern Recognition Digital Computer with Application to the Automatic Scanning of Bubble Chamber Negatives," by B. McCormick and R. Narasimhan.

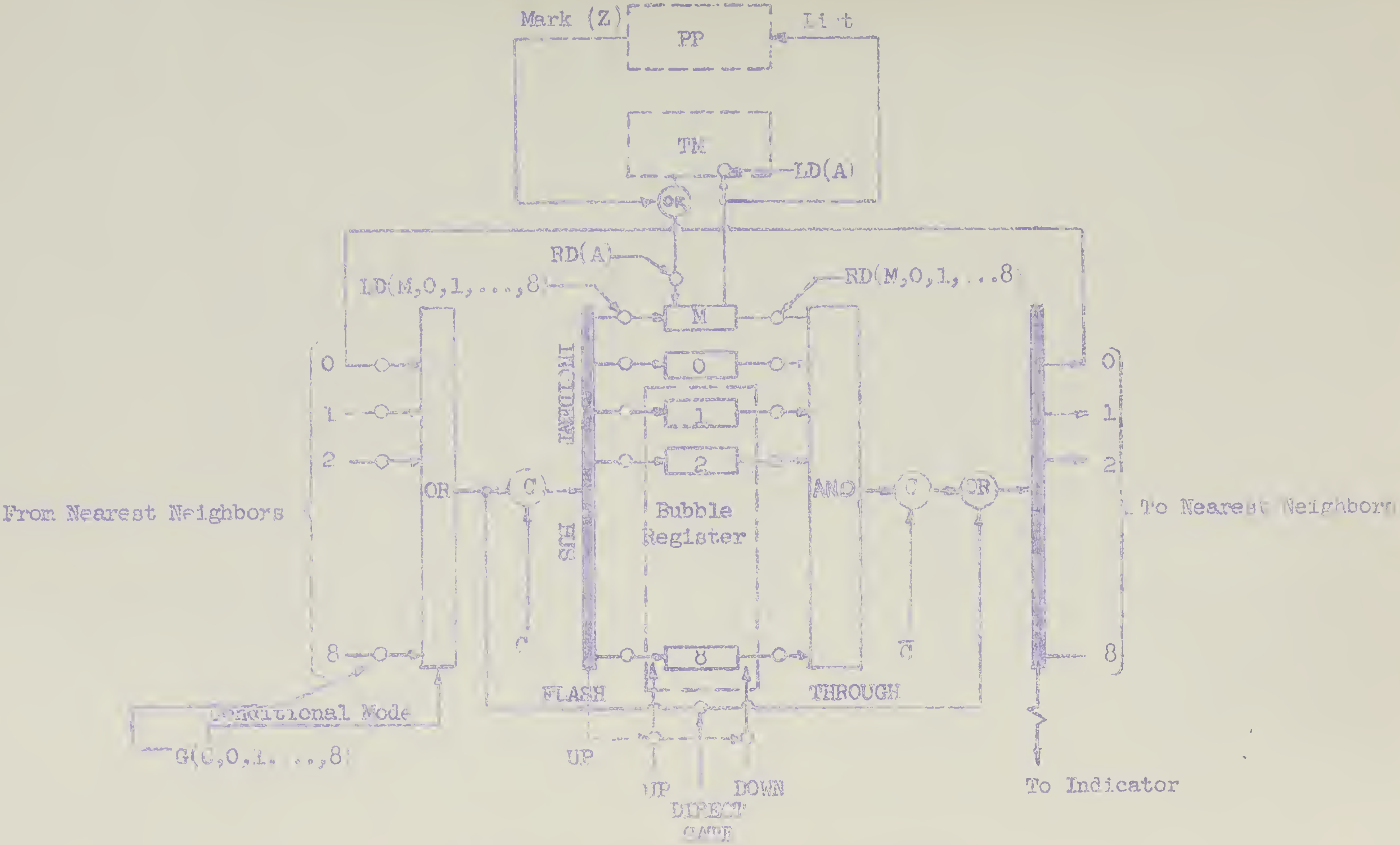

FIGURE 1. SCHEMATIC OF [illegible] [illegible]

1.2 STALACTITE SIGNAL FLOW

Each input to the stalactite, including one representing the state of its own output, is individually selected by INPUT SELECTORS. This selection may be made conditional or not on the contents of a corresponding flipflop, depending on the setting of the CONDITIONAL GATE line. In either case the result of selection is fed to an INPUT OR circuit, whose output may be gated via a COMPLEMENTER to the bank of ten flipflops or alternatively bypassed to the OUTPUT OR. The signal is gated to any or all of the eleven destinations by the actuation of a gate control line common to all stalactites.

The required fanout and double gating of the flipflops is achieved by FLIPFLOP SIGNAL DRIVERS implied by the INCIDENT bus labelled in Figure 1.

The output of any flipflop may be selected and combined in an OUTPUT AND. The resulting information passing through the OUTPUT COMPLEMENT circuit may be complemented or not before being combined with the bypass from the input in the OUTPUT OR. The resulting signal feeds an OUTPUT DRIVER which in turn feeds the output lines.

Besides the normal gates on all flipflops and the cable driven entry to the M flipflop, an additional set of BUBBLING GATES can control eight of the ten flipflops as a BUBBLING REGISTER.*

1.3 THE BUBBLING REGISTER CONNECTION

The BUBBLING GATES are controlled by UP and DOWN drivers which may be operated separately or simultaneously. In the restricted case that only time-separate actuation of the UP and DOWN drivers is allowed, the register is limited to the stacking operation only and the mechanism is termed STACKING GATES. In either case the action of the gates is inhibited by a zero on the INCIDENT BUS. Provided this bus is a one, the UP gate controls the transfer of information to a receiving flipflop from its neighbor below (having the next lower index) while DOWN controls transfer to a flipflop from its neighbor above. A truth table description of the required operation for separate UP and DOWN pulses is shown in Figure 2. In the event of an UP

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* Report No. 122.

Initial State			Effective Drive	Final State After Simultaneous U and D	Comments	Final State After U Alone	Final State After D Alone
A	C	B		B'		B'	B'
0	0	0	U	0	Gate to Zero	0	0
0	0	1	D	0		0	1
0	1	0	Neither	0	Leave Alone	0	0
0	1	1	Neither	1		1	1
1	0	0	U/D	1	Reverse	0	1
1	0	1	U/D	0		0	1
1	1	0	D	1	Gate to One	0	1
1	1	1	D	1		1	1

pulse the receiving flipflop is gated to a 0 if its neighbor below is 0 and is otherwise left alone. In the event of a DOWN pulse the flipflop is gated to a 1 if its neighbor above is a one. The end conditions are equivalent to a "phantom" neighbor which will always gate the adjacent flipflop. If the flipflops are called A. B, C in descending order then in the event of a DOWN pulse B becomes $B' = A \vee B$ while in the event of an UP pulse B becomes $B'' = BC$.

In the simplest implementation of the desired Stacking action for separate UP or DOWN pulses it does not matter in which state the "receiving" flipflop already exists. If a gate to 1 should occur for example, the flipflop changes if it were originally 0, but though gated, stays the same if it were already a 1. However, if both UP and DOWN pulses are applied simultaneously, the receiving flipflop is subjected to conflicting demands for its final state. But if the gating acting is made conditional upon the state of the receiving flipflop, such that it receives no gate if it is already in the state to which the gate would force it, then the behavior known as Bubbling* will result. Figure 2 gives a truth table for the behavior and Figure 3 illustrates the effect graphically.

In summary, upon simultaneous application of both UP and DOWN pulses, three cases may be distinguished depending on the response of the receiving flipflop to the pulses applied separately. a) neither causes reversal, b) only one causes reversal, 3) either causes reversal. Simultaneous application of both UP and DOWN will reverse the receiving flipflop in cases b, c but will leave it unaffected in a.

This discussion has thus far treated a single receiving flipflop gated on the basis of information from two adjacent flipflops. If these other flipflops are also a part of the same Bubble Register then they, too, will be gated by the UP and DOWN pulses and some difficulty may arise in determining the final state.

I.4 THE REQUIREMENTS OF A WORKING REGISTER

Though the required Stacking response to widely separated UP and DOWN pulses can be implemented in several fairly simple ways, the major

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* File No. 463, Report No. 122.

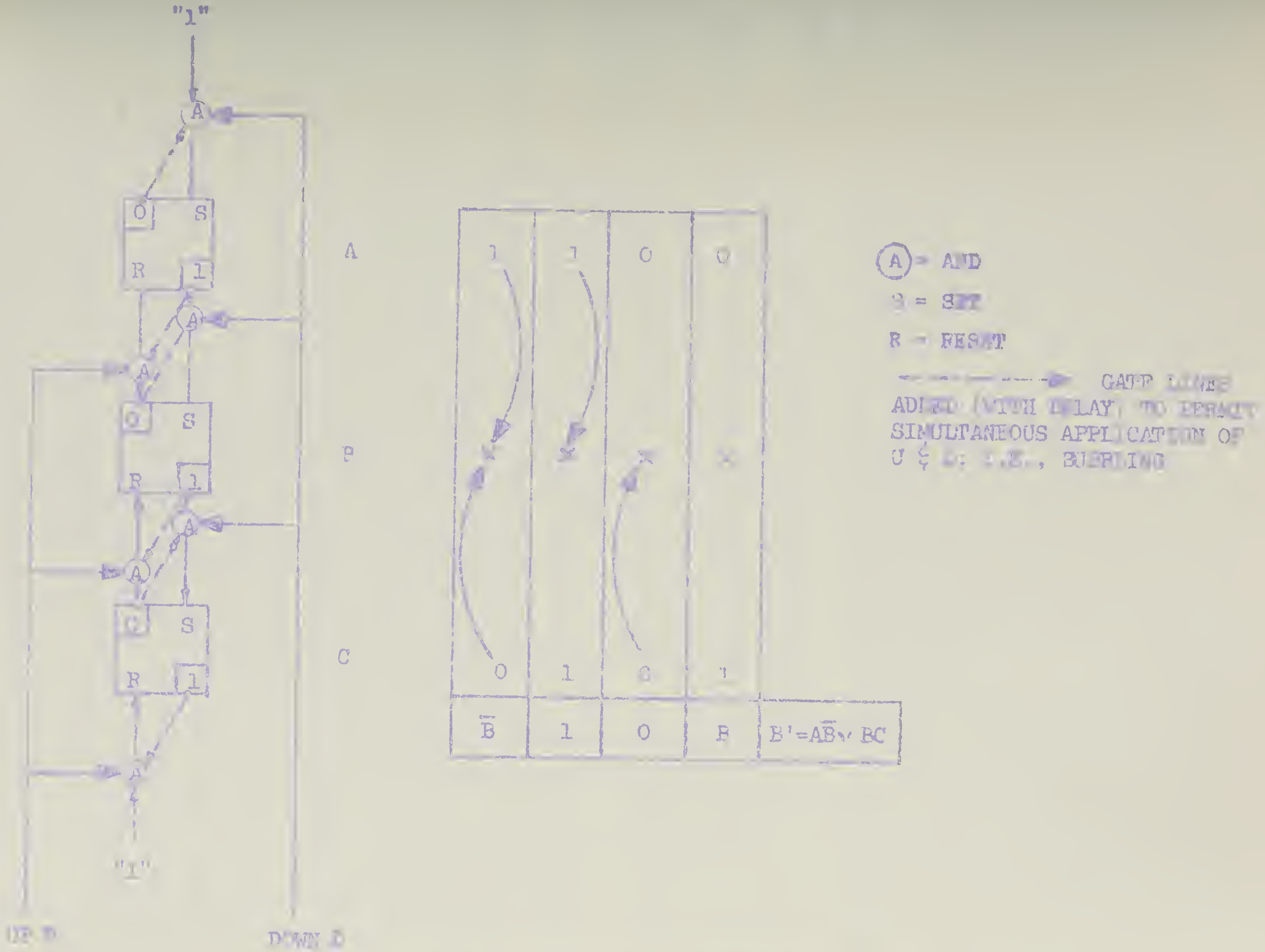

FIGURE 5 LOGICAL REALIZATION OF [illegible] REGISTERS

requirement in such is the temporary storage of a previous simple state, viz. the 1 state of flipflop A when gating DOWN at 5, or the zero state of flipflop C when gating UP at 7. The extremely direct relationship of the stored information to the state of the flipflop will imply, in any possible circuit implementation a relatively direct gating connection to the temporary storage element. Thus it would seem possible, and it is in fact true, that the energy required to change the state of the storage element can come directly from a flipflop output. Thus in the present case where high-speed operation is desirable and when the required energy is large the speed is limited directly by the design of the flipflop, its current level and load-handling capability.

This simple situation is to be contrasted to the case in which the Bubbling response to "simultaneous" UP and DOWN pulses is required. Here, as will be shown, temporary storage of a doubly conditioned previous state is necessary, and the required logic shall necessitate some compromise between speed and circuit complexity.

It is convenient to compare the simultaneous Bubbling case with the problems of design of simple, capacitor-driven, commutating, binary counters. One must be sure in both cases that part way through a transition induced by one of the inputs that the flipflop is not loaded or "second-guessed" by the other input. In the most naive counters this problem is skirted by making the drive pulse about equal to the flipflop regeneration time but short compared to its settling time. The flipflop's memory of its previous state stored in the commutating or speed-up capacitors helps ensure that the flipflop once switched will settle in the state opposite to that in which it began. More sophisticated counters view the gating action as providing additional memory of the flipflop's initial state, in an initial charge in one of the gating capacitors. Since this initial charge must be established before gating is again possible, false triggering due to long drive pulses is obviated.

The same problem of false retriggering is found in the Bubble Register design for the case of simultaneous inputs. Here, also, it will be necessary to provide temporary storage of the previous flipflop state as well as the state of adjacent flipflops, to the extent that these are concerned.

will gating the particular flipflop be possible. However, [illegible] as used, the conditions involved in gating either side of a particular flipflop, it appears that only a single storage element incorporating a [illegible] condition, as "gate" or "not gate," is both economical and simplifying. Henceforth the adjective "primed" when referring to the gate or storage element shall indicate that both the source flipflop (from which information originates) and the receiving flipflop (to which information [illegible]) [illegible] to the correct condition for a drive pulse (either UP or DOWN) to produce a change of state in the receiving flipflop.

11.0 DESIGN OF STACKING LOGIC

Figure 1.[illegible] illustrates a gating connection to a standard flipflop which will perform the required logic for the stacking operation. The circuitry is simple and conventional, being related to that used in commercial binaries and identical to that used in simple shift register design.

11.1 MODE OF OPERATION

The gating information on temporary storage of the state of the controlling flipflop, say A, is stored in capacitor C_1. In the quiescent state, with UP and DOWN drivers off, C_1 is charged positive through [illegible] if A = 1 or is charged negative via R_1 if A = 0.

During a DOWN drive for which a [illegible] volt positive pulse is applied by DOWN bus, the conducting state of D_2 will depend on the previous storage on C_1. It will conduct and force the flipflop down condition if A had been 1 and otherwise remain cutoff. If during this same pulse, the state of A flipflop is also changed, the operation on B is unaffected due to the storage on C_1 and the existence of D_1.

[illegible] Circuit Design

The Flipflop

The flipflop has been designed using "worst case" type design for which a power supply tolerance of ± 5% and resistor tolerance ± 1% have been used. Both $\overline{V_{BE\,sat}}$ and $\overline{V_{CE\,sat}}$ have been taken to be 0.5 volts. The resulting maximum drive-capability of the flipflop is about 1 ma. for a β_{min} of 20. Part of this will be used in driving the positive capacitor C_1 in the next flipflop.

Though the precise details of the way in which C_1 is charged positive depends on the design of the line driver, the peak current for this purpose is an important consideration. The magnitude of the available [illegible] current depends on the transistor β, the value of the speedup capacitor C_s, and the size of the collector resistor. Though the speedup capacitor is conventionally, and in this case also, used to remove stored charge from the transistor during turnoff, it also provides in this case the 10 to 20 ma. required to charge C_1 during the flipflop regeneration time. The precise value depends on the design of the drive, and on the transient behavior of the flipflop.

Gate Capacitor

The value of R_1 and the voltage to which it returns are critical in determining the recovery time or the zero-charging time of C_1. This time is also a strong function of circuit tolerances, being at least dependent on the maximum size of the line drive pulse and the minimum sensitivity of the flipflop to small current pulses. If R_1 is returned to -12 volts it gives a more nearly linear discharge and for a given discharge time represents less peak load on the driving system. However, the current in R_1 to -12 volts must be supplied from the neighbouring flipflop while it is in the zero state, and if too large may falsely trigger that flipflop. It appears at present that an R_1 = 1.5 k connected to -6 offers a reasonable compromise with adequate recovery [illegible] in the time constant of 1.5 × C_1 µsec.

Diode D_1 is used only to charge C_1 positive from flipflop 1. It should have no direct effect on flipflop 2. In order that no current flows through diodes D_1 and D_2 in the event that $V_{CE\,sat}$ of 2 is small and $V_{CE\,sat}$

of 5 ma large it is necessary that D_1 be silicon with a specified drop at 1 ma of > 0.4 volts while D_2 can be germanium with a drop < 0.3 volts at 100 ma. Thus even in the worst of Vce_{sat} = 0.3 volts and Vce_{sat} = [illegible] the drive on the flipflop base will not exceed 100 ua.

The Storage Capacitor

The minimum DOWN pulse which the driver of Figure 2-11 will produce is 3.8 volts. The minimum pulsed voltage at the D_1 - D_2 node before gating results from the maximum diode drop and Vce_{sat} voltages. It may be as low negative as - 0.6 - 0.6 = - 1.2 volts. Thus when the DOWN pulse is applied this node will tend to go at least to +2.6 volts and the base of the flipflop transistor shall tend to + 2.1 volts.

In order that the flipflop be gated properly its base must be held above ground for the regeneration time of about 20 nsec, supporting the load of R_1, after supplying the charges to D_1, the transistor base and the [illegible] speedup capacitor. Thus for a DOWN drive rise time of < 20 nsec, the current in R_1, about 4 ma. must be supported for about 40 nsec. Thus C_1 must supply ~150 pc for this reason. The stored charge in D_1 is < 25 pc and that in 2N960 series transistors with these operating conditions is < 100 pc. The charge required for a 0.5 volt change in 27 pf is 15 pc. Thus, the total charge transmitted by C_1 must be less than 300 pc, and C_1 = 150 pf should be adequate in view of the minimum 2.1 volts available.

Under the previous conditions one should investigate the recovery period which must be allowed between the finish of one UP/DOWN pulse and the next. The maximum drive pulse available from the driver of Figure 2-11 depends on the -6 volt supply. The pulse varies from 4.8 to 5.4 as the supply covers the range - 5.7 to - 6.3. In order that the flipflop be unaffected by the drive pulse the capacitor voltage must begin sufficiently low that it will not cause D_2 to conduct even with the largest transistor base voltage. Thus the C_1 - D_2 node must remain below -0.6 + 0.2 or -0.4 volts and must therefore have been below -5.2 or -5.7 (depending on the supply voltage) before the DOWN pulse can be safely applied after a previous gating of the flipflop. Thus the C_1 - D_2 node must recover about 90 percent of the total swing, a feat which can be accomplished in about 2.5 time constants or some 500 nsec.

A faster, though more expensive design is possible using clamp diodes to -6 volts in the flipflop collectors. In this case R_1 can be returned with no danger to -12 volts to produce a much faster capacitor recovery.

III.0 DESIGN OF BUBBLING LOGIC

Figure 2-7 illustrates gating connections to a standard flipflop which will perform Bubbling logic. This circuit embodies an extension of the ideas described in connection with the Stacking Logic circuit design.

III.1 MODE OF OPERATION

As in the case of Stacking Logic design, capacitor C_1 provides the temporary storage of the priming information, which, however, in this case is a function of the states of both the flipflop to be gated, B, and its neighbor, A. Because of its two binary inputs C_1 is required to store information related to four states, only one of which, the primed state, indicates that the flipflop will reverse in the event of a DOWN pulse, say. Referring to the voltage level of the nodes U and L at the upper and lower ends of capacitor C_1, the gate conditions can be summarized as in Table 1.

TABLE 1

	Input from Adjacent Flipflop (A)	Input from Gated Flipflop (B)	Node U	Node L	
1)	-	+	-	+	unprimed states
2)	-	-	-	+	
3)	+	+	-	-	
4)	+	-	+	-	primed state

In the event of a positive going DOWN pulse case 4 or the primed case is the only one for which conduction of D_2 and gating of the flipflop should occur. In cases 1 and 3, D_3 does not conduct since node U is held positive via D_4 while in case 2, though D_3 conducts, node U has been negative and the added pulse voltage at U will be insufficient to cause D_2 to conduct.

III.2 CIRCUIT DESIGN

The Flipflop

The flipflop design is similar to that used with Stacking Logic, though the load-driving requirements are more stringent. Each flipflop must support a minimum static load consisting of its own R_2 and the R_1 of the adjacent flipflop. The transient load present during the charging of C_1, is limited but may assume various values depending on the particular states of the flipflops.

The worst case occurs when the flipflop is gated directly by the signal gates shown in Figure 2-7, at a time when flipflop A, being a 1, is supporting the current in R_1 and flipflop B being a 1 has released the current in R_2. The maximum current, partly coupled through the storage capacitors of A and B will be approximately $(12 + 6)/R_2 - 6/R_1 + (6 + 6)/R_1 + 12/R_2$ for the -6 and 12 volt connections to R_1 and R_2 shown. Though, as in the case of the Stacking logic design, the speedup capacitor C_2 is of some help, the charging rate of C_1 will be sufficiently slow as to require the major part of this current as static load-carrying capability in the flipflop.

Gate Components

The static design of the gating elements follows generally the same ideas as have been demonstrated with the Stacking Logic design. For the same reasons as previously stated D_1 is a silicon diode. A silicon diode is also used for D_4 where the added drop at very small currents allows the driver system to support a larger part of the load of R_2 than it might otherwise do.

The Storage Capacitor

A tolerance design for the determination of the value of capacitor C_1 will not be given here due to its length. The details are similar [illegible]

to those discussed previously, though the existence of additional components in the driving path via D_3, introduces sufficient variability that a conservative worst case design does not seem advisable. The penalty for accommodating the unlikely event of accumulated tolerance would be greatly reduced speed in normal operation. As this seems to be a large price to pay the recommended design will fail the usual worst case transient analysis. Though a value of C_1 of 150 pf has been recommended, capacitors of one third this value were found satisfactory on a small scale test. The time for recovery of capacitor C_1 before Stacking/Bubbling operations can proceed is estimated to be about 500 nsec.

IV.0 DIRECT AND CONDITIONAL INPUT GATES AND INPUT OR

The two designs shown in Figures 1-1 and 2-1 for this function are similar in their use of diode input logic, and differ mainly in the technique of level shifting used. Gating is controlled by a separate diode gate for each signal input as well as by a CONDITIONAL GATE CONTROL (Figure 1-1 and 2-2) which provides one of a pair of mutually exclusive signals to each input gate via resistors. With this control set to DIRECT, gating is straightforward. With the control set to CONDITIONAL, another level of diode logic is caused to operate making the input gating additionally conditional upon the state of the corresponding register flipflop.

The result of gating a negative "1" is a negative voltage fed to the last stage of diode logic where a negative OR function of all gated inputs is formed and amplified.

IV.1 CIRCUIT DESIGN

The current level in the diode logic is established by the choice of the resistor labeled R_1 in Figures 1-1 and 2-1, which determines the minimum positive driving capability of the diode logic. Once this choice is made the negative driving characteristic must follow. It is intrinsically true that a design able to support some minimum load at the negative extremity

will supply considerably more current when tolerances are nominal or at their other extreme. This excess current, though perhaps unnecessary, must be supported by various gates, clamp diodes, saturated bases, etc., and in this way is a powerful influence on the rest of the design. The excess current can be reduced if the load driving capability of the logic in the negative direction is reduced, or alternatively it can be used to advantage—in the present case to increase speed of operation. The former approach is followed by the circuit of Figure 1-1, the second by that of Figure 2-1.

In Figure 1-1 an emitter follower is used to drive the output inverter, supplying it a large turnon drive, limited by the diode negative feedback, and controlling the turnoff drive from the 2.7K resistor to +6 volts. The base of the emitter follower is quite easy to drive, certainly in a static sense, and will require virtually no DC base current. Thus, the 8.2K resistor to -6 volts is used to supply leakage and stray capacity for positive going signals and represents the only static load for which the rest of the circuit must be designed.

In Figure 2-1 an NPN inverting circuit is used to drive the first output transistor. Though this configuration has considerable current gain it still requires a large static base current. This and various stray effects are supplied by the 5.1K resistor to +6 volts. The logic must be able to pull negative on the 5.1K as well as supply excess current for transistor turnoff. Since the voltage swing at the base is limited by the conducting base and a bumping diode, charging of stray capacitance is not too important. Though the logic as designed will supply only 0.5 ma of turnoff current in the worst case its nominal operation, and thus typical speed will be much improved.

V COMPLEMENT CIRCUITS

Complement circuits (Figures 1-2, 1-7, 2-4, 2-11) are interposed in the signal path between the INPUT OR and flipflop gates and between the OUTPUT AND and OUTPUT OR circuits. Their function is the usual one of providing either the input signal, I, or its complement as an output, O, under control

of [illegible]

[illegible]

Complementers of Type 1 and 2 differ somewhat in circuit detail though the input and output complementers of each type are virtually the same. Each of the designs is based on ±5% power supplies, ±10% resistors, $Veb_{sat} = Vec_{sat} \leq 0.6$, $v_{diode} \leq 0.6$ and a minimum β as indicated adjacent to the transistor in the figures (either 20 or 30). In circuits of Type 1 over-current is supplied to a large degree by the speedup capacitor of [illegible] pf. In those of Type 2 a speedup is not used, though the current levels could be reduced somewhat if it were. Because of the simple drive used in this case and the loading effects of the capacitors on the drive circuit as it falls negative, a smaller speedup capacitor < 20 pf would be most satisfactory.

VI. OUTPUT AND CIRCUIT

The OUTPUT AND Circuit shown in Figures 1-7 and 2-10 are identical directly to parts of the INPUT OR circuit of the same type. Since a negative OR doubles as a positive AND, the notation is consistent with positive "1"'s available from each flipflop's zero side output.

Because of the simpler gating logic required, the diode gate input used in the INPUT OR can be replaced by a gate signal on the gate resistor. This simplification was not available at the input due to the need for conditional gating. The external community gating drivers used, can be identical to the input part of the CONDITIONAL GATE CONTROL of Figure 2-7.

VII. UP AND DOWN DRIVERS

Bubbling Logic and to a lesser extent Stacking logic requires UP and DOWN drive signals of well-controlled amplitude, duration and rise time.

circuits for this purpose are shown in Figures [illegible] and [illegible], where the differences are related only to the input requirements of Type 1 and Type 2 circuits.

The signal output levels are controlled by saturating transistors and diode clamps where necessary. Regeneration, designed to operate as soon as the output signal begins to move positive, ensures a fast-rising edge. The regenerating capacitor also serves the purpose of pulse stretching so that the minimum length of the UP and DOWN driver can be assured by this means.

Diode inputs to the base of the output transistors allow the zero signal at the output of the INPUT COMPLEMENT circuit to inhibit the application of the UP/DOWN drives.

In order that the UP and DOWN drives be as nearly possible simultaneous for Bubbling Operations, a separate driver used to gate both UP and DOWN is incorporated.

VIII. CABLE DRIVERS AND TERMINATORS

A cable driver and a cable termination gate is required for output from and input to, flipflop M. Circuits for these purposes are shown in Figures 1-8, 1-9, and 2-9.

The cable to be used has a 93 ohm nominal impedance and is matched at the receiving end by a 91 ohm termination. During the time for which the cable driver is on, the sending end is also matched. Signals of 2 to 3 volt nominal amplitude are transmitted in this way.

Two basic designs of terminators are shown. The diode-coupled design of Figure 1-9a presents only a small loading of the cable when gated and a negligible loading when not. Thus it may be used for multiple taps on a long cable if need be. The transistor-coupled design of Figure 1-9b presents a somewhat greater load to the cable which depends on the precise circuit configuration (Figure 1-9c). In the worst case shown the load may be as small as 300 ohms during gating but this should not cause serious reflections.

IX. TRANSISTOR GATE DRIVERS

The gate drivers required by the stalactite board are many and varied. The majority of these drive resistor gates negative through a [illegible] to 9 volt swing, some operate via diodes at standard signal levels, while a single one used for flipflop gating in Type 2 circuits must go from zero to +5. Though the detailed designs are incomplete as yet and are not included in this report, they are generally similar to circuits which have been described, namely the Conditional Gate Control, Flipflop Signal Drivers, the Output Driver, etc.

By the use of currently available, medium power, silicon, npn transistors like the Motorola MM 488, semi-saturating drivers capable of 200 or 300 ma are easily designed, giving a fanout of perhaps 20 or so in the worst case. Because of the reasonably small fanout there should be no need for special cable or termination resistors.

Gate signals which are fed through diodes in the manner of logic signals constitute a rather special problem with respect to noise allowance. The noise margin allowed in the logic is small and consistent with the short distance over which a signal must travel from one stalactite board to the next. Gate signals on the other hand are less local and problems of inter-ground noise voltage, etc.. may exist. This is particularly important for the positive swing of signals derived from grounded emitter amplifiers. Accordingly the positive signal swing of this type of gate should be extended to about +1 volt or so.

X. EXPERIMENTAL VERIFICATION

Thus far, a complete Stalactite board has not yet been assembled. However, tests have been made to varying degrees on various component parts. The greater part of the effort thus far has been spent on developing an adequate Bubbling Logic system. The complexity of this part of the stalactite alone makes it extremely difficult to perform complete tests without a complex logical control. However, considerable success has been had using three and four coupled flipflops and special purpose test-pulse generating equipment.* Since the complete findings of these experiments will be reported on elsewhere, a brief description of the measurement techniques and some results only will be described here.

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* Test equipment has been fabricated and tests performed by D. C. Hall.

A test pulse program was evolved in which a group of UP pulses could be alternated with a group of DOWN pulses. The number of pulses in each group was variable as was the overlap of the pulse trains. By adjustment of the overlap an alternating set of UP and DOWN pulses could be preceded by some adjustable number of either alone. During the blank period between pulse groups the flipflops could be reset to any desired initial state. Thus it was possible to controllably repeat some pulse sequence of interest while observing flipflop behavior. Of course, in addition to the possibility of alternating pulses, overlapping pulse clocks were easily generated. In this way the response of the register to "simultaneous" pulses could be observed.

Initial experiments were done on several different designs of Bubble Logic on which the final design of Figure 2-7, for example, is based. The designs for which most data is available differed from that of Figure 2-7 in the respect that the impedance level was generally higher by perhaps 50 percent and the storage capacitors were disproportionately lower. There is no very valid reason, in hindsight, for lowering the impedance level of the circuit to that of Figure 2-7. A marginal improvement in speed, less noise susceptibility and increased power consumption seem to be the only important factors.

Measurements on the prototypes indicated that simultaneous operation was possible for UP and DOWN drives coming within 60 nsec of each other and that alternate pulse operation was guaranteed for pulses farther than 270 nsec apart, using a 70 nsec pulse width. This measurement compares reasonably with the critical time constant of about 300 nsec for the particular circuit. The flipflop settling time measured from 10 percent in, to 90 percent out of the last moving collector was 65 nsec.

Though some confidence has been achieved by measurements of this limited sort, no means is presently available for detecting false operation which may occur randomly and/or at a low rate. A device is about to be constructed, with similar circuits to those already used, to make clock pulse generation conditional upon the correct flipflop having operated during the last clock pulse. Thus when the cycle stops due to failure the offending flipflop and triggering condition may be detected.

[illegible] [illegible] of the [illegible] [illegible] was [illegible] to measuring the function of the DIRECT TRANSFER or FLASH-THROUGH operation in response to various [illegible] at the input to the INPUT OR in Type [illegible] circuits. Fast signal propagation in this path is particularly important in the system design.

It was found that for all possible conditions of [illegible] inputs to the INPUT OR including the total operation time of the CONDITIONAL GATE driver, the maximum time for 50 percent input to 50 percent of the output of the OUTPUT DRIVER was less than 93 nsec. The operation time of the INPUT OR was measured to be about 40 nsec from 50 percent input to 50 percent output. These measurements were taken with a single input [illegible] reverse biased diodes to duplicate other inputs. The OUTPUT DRIVER was not loaded, though measurements were made with three 11.5 pf probes on the output of the INPUT and OUTPUT OR's and the OUTPUT DRIVER

Conclusions

Designs have been illustrated for the [illegible] circuit implementation based on two design philosophies. However, a decision bearing on the relative merits of the two circuits must await further large scale tests.

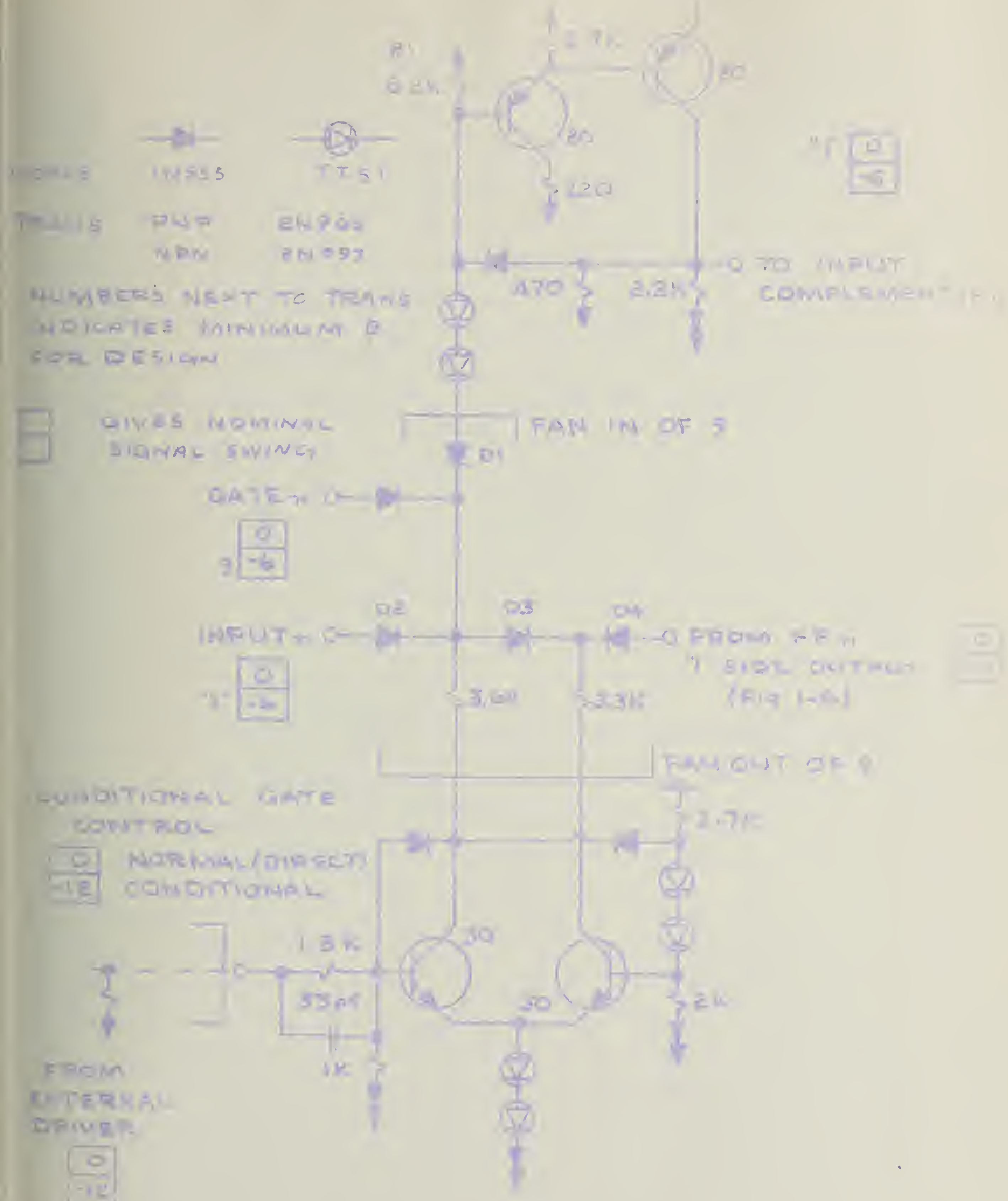
The DIRECT TRANSFER or FLASH-THROUGH operation has been shown to be quite fast (< 9[illegible] nsec) with Type [illegible] circuits. This would indicate that perhaps a reduction in circuit current levels might be possible while maintaining adequate speed. Such a setting [illegible] operation would require further research.

Estimates based on measurements of isolated sections of Type [illegible] circuits indicate that the signal progression from the input, through [illegible] flipflops, and to the output should be about [illegible] nsec.

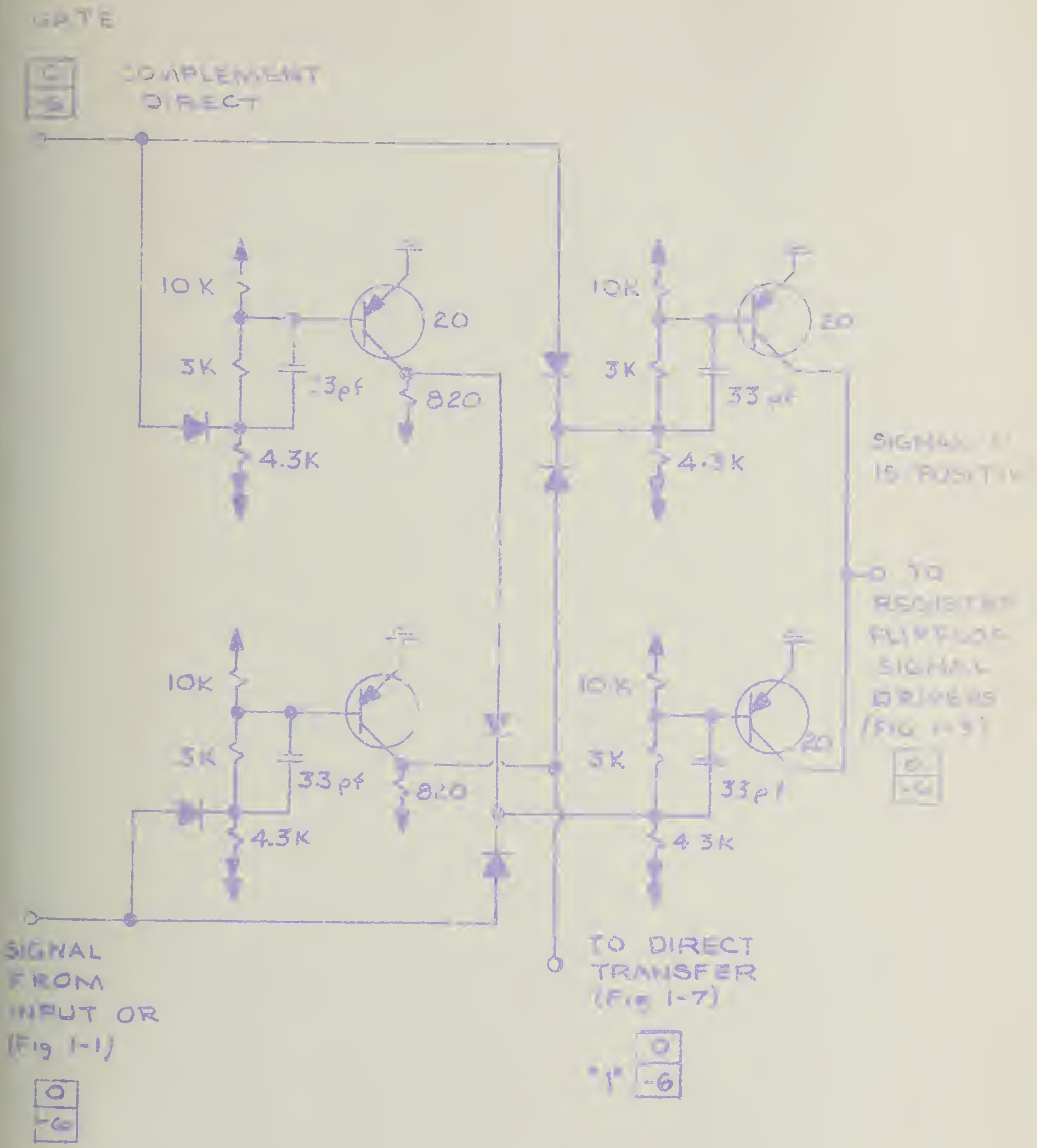
A complete subtractor with [illegible] logic can be implemented with [illegible] transistors, 24[illegible] diodes, 2[illegible] resistors and [illegible] capacitors in Type [illegible] circuits. If [illegible] logic alone is used, [illegible] transistors, [illegible] diodes, [illegible] resistors and [illegible] capacitors would be needed.

If the Q flipflop and CONDITIONAL GATE CONTROL were removed, if the conditional Gates in flipflop [illegible] were eliminated and if the [illegible] [illegible]

[illegible] of the output unit [illegible] transistors, 20 diodes, and 20 resistors could be made. The expense, however, would be [illegible] reduction in reliability.

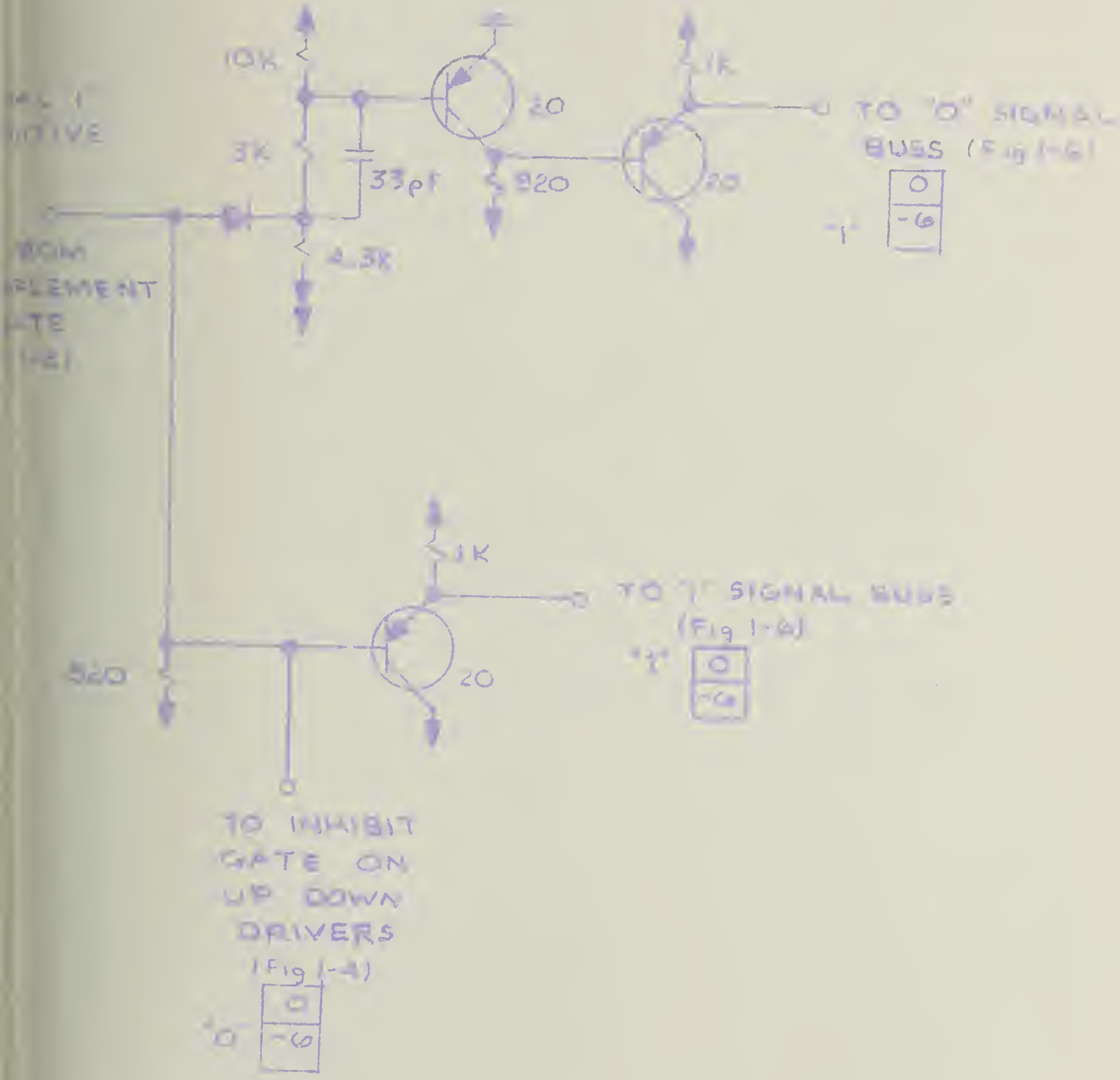


INPUT OR AND GATES WITH DIRECT AND CONDITIONAL CONTROL
Fig 1-1



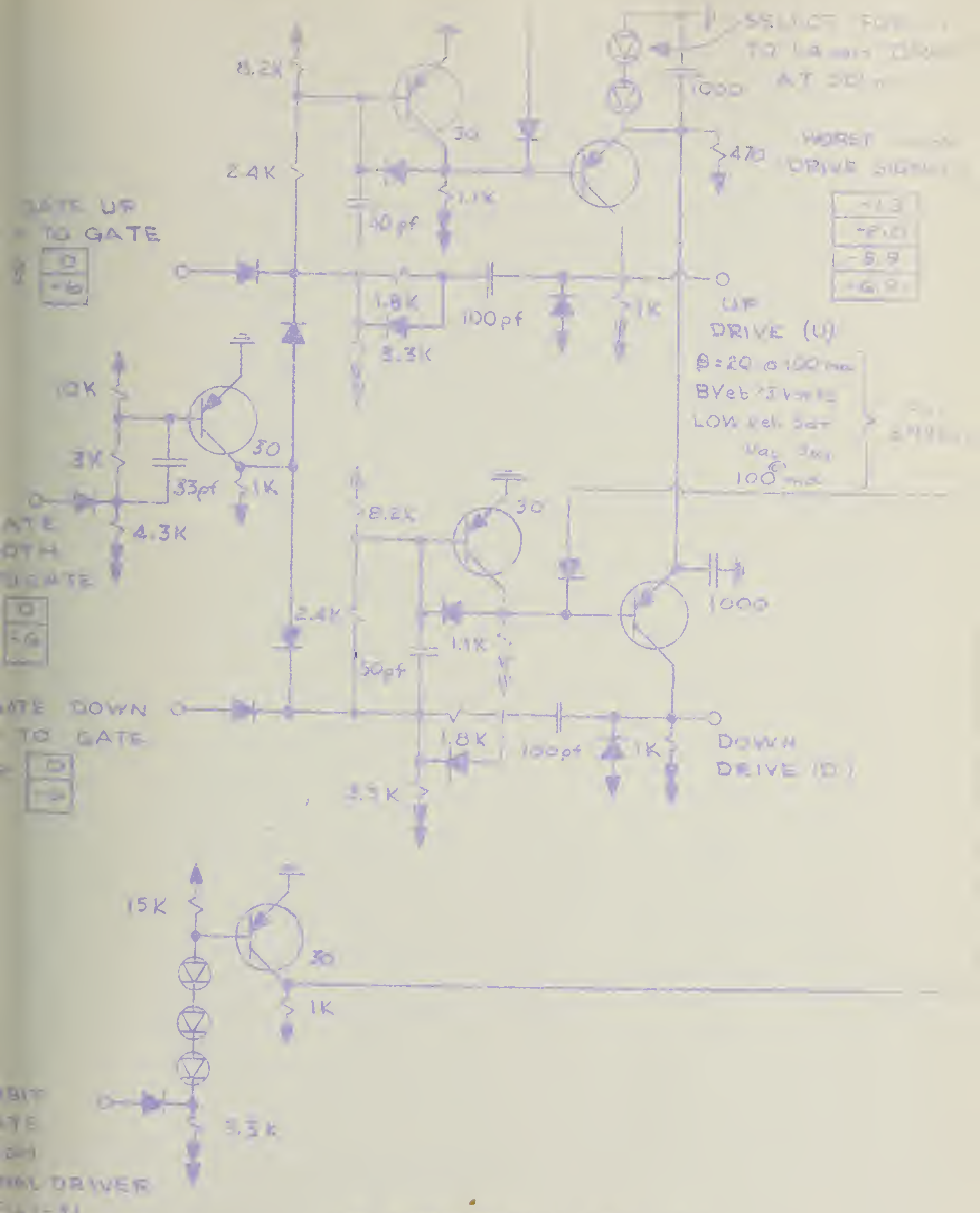
INPUT COMPLEMENT GATE

Fig 1-2



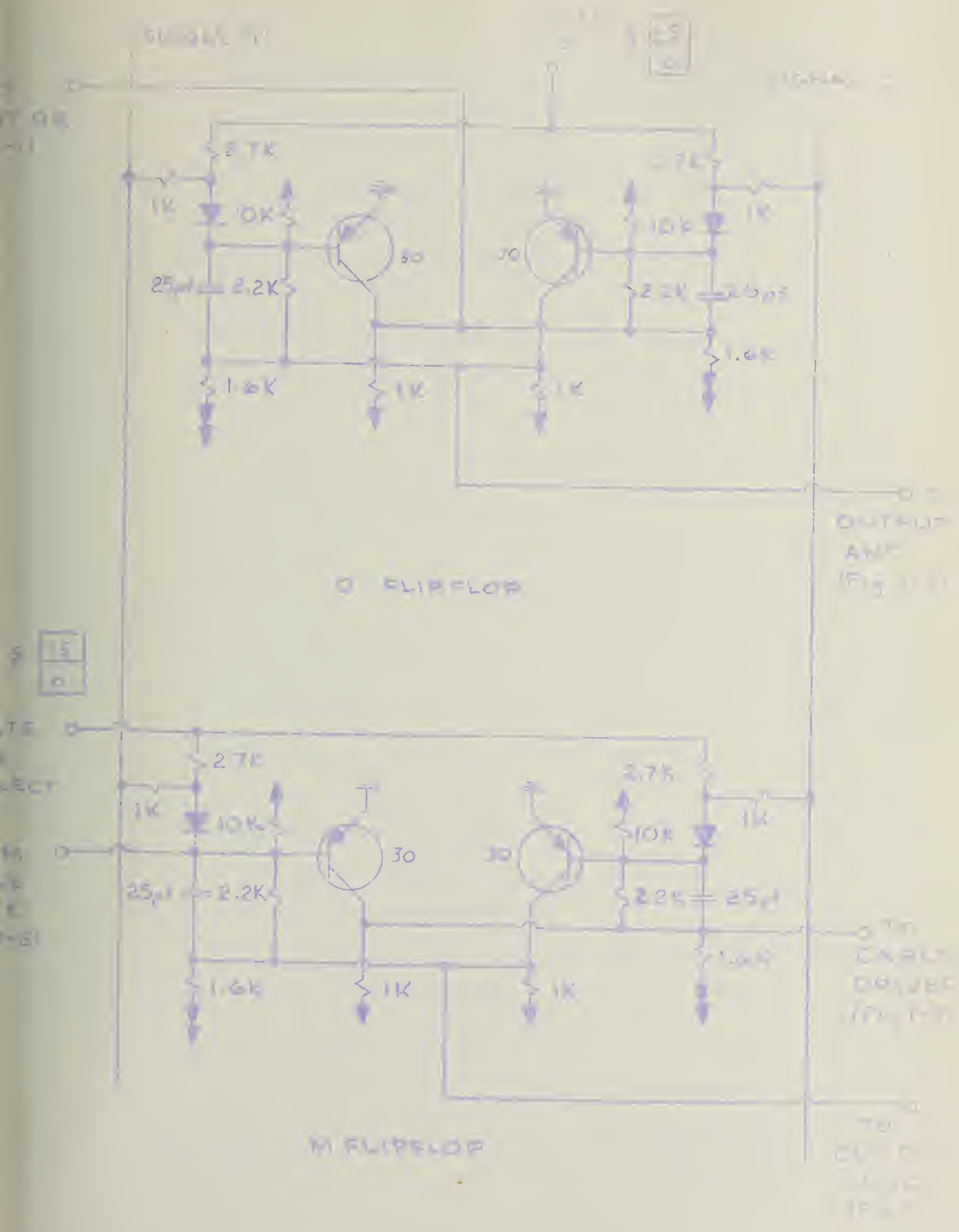
REGISTER FF SIGNAL DRIVERS

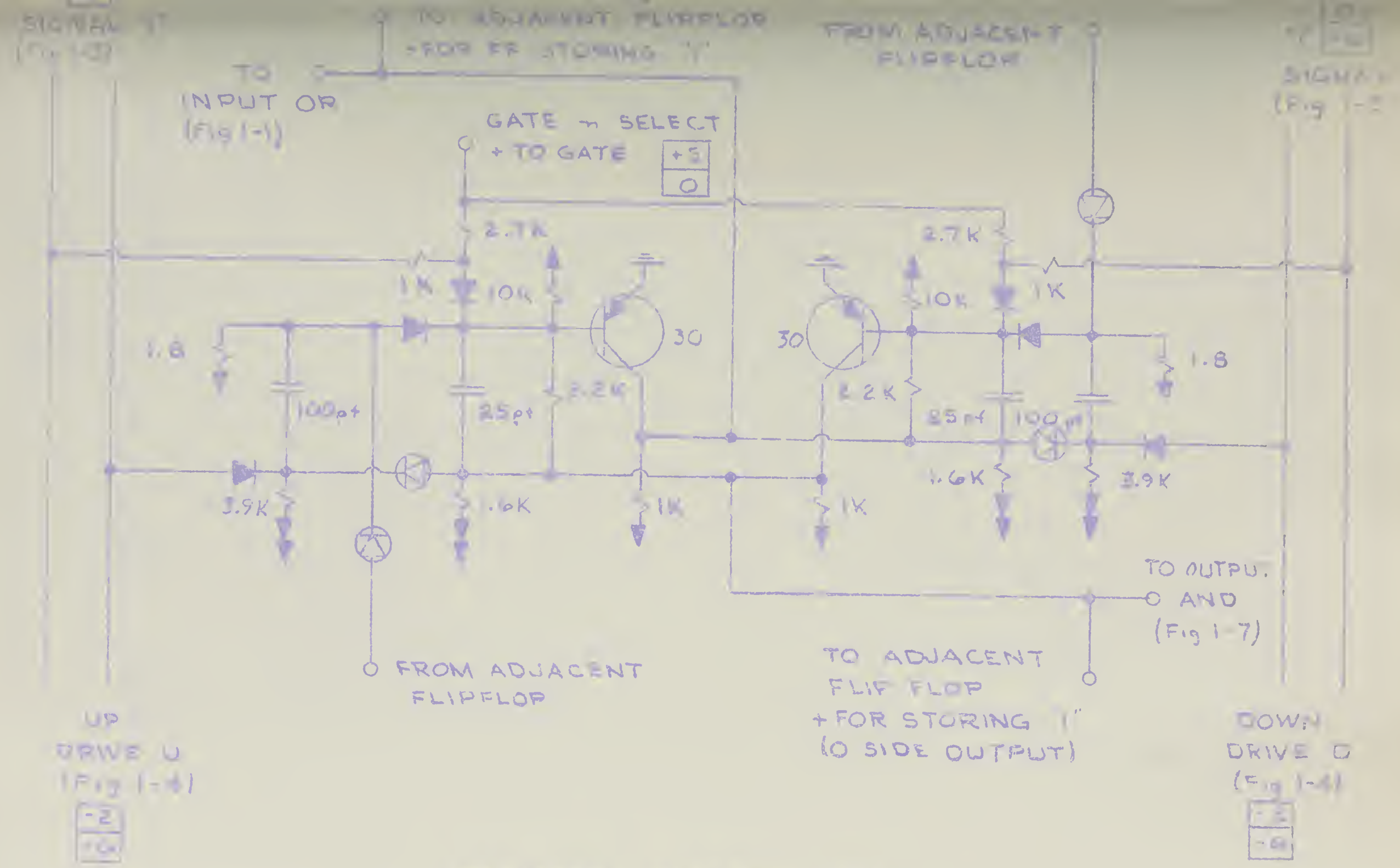
Fig 1-3



UP AND DOWN DRIVERS

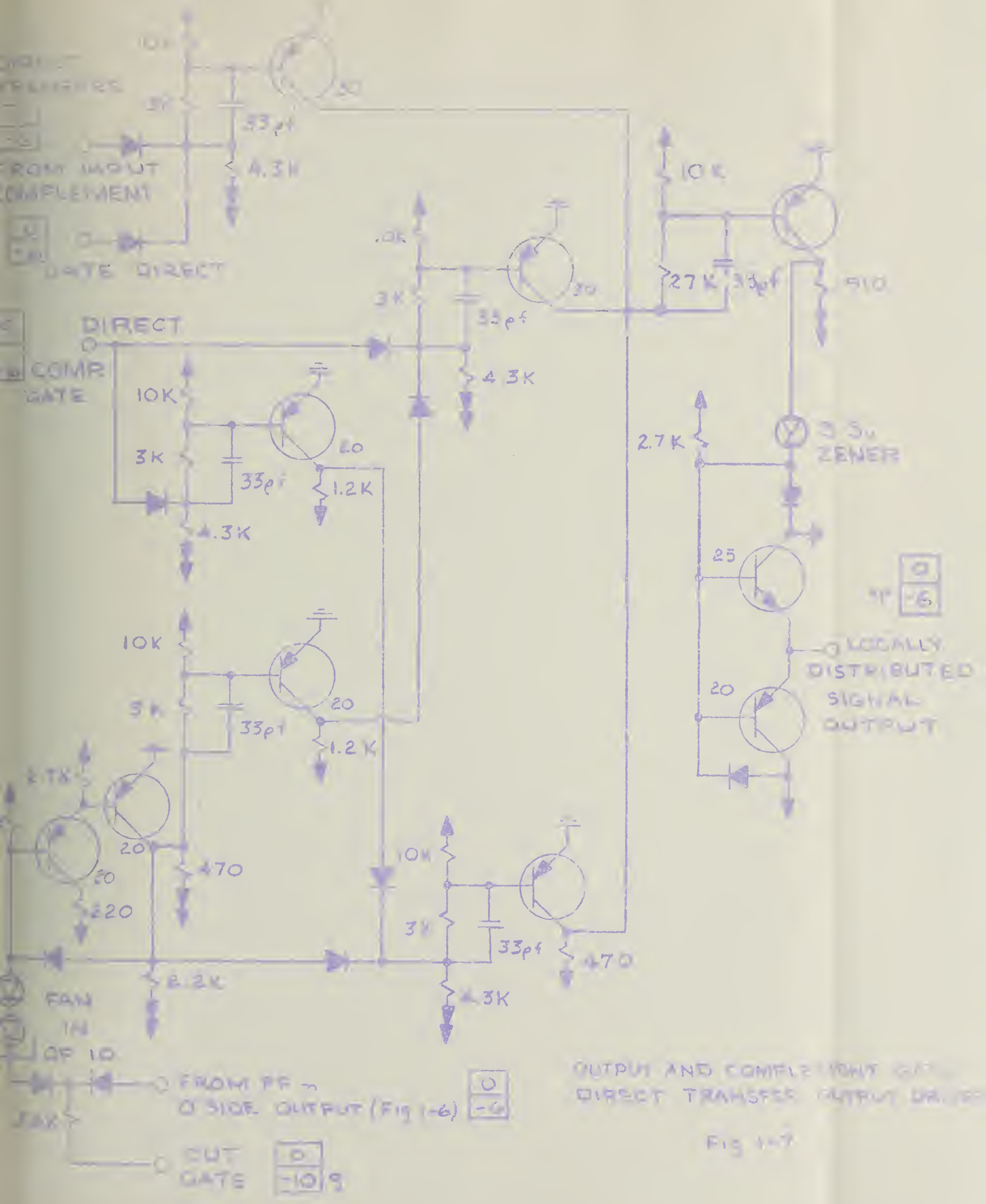
Fig 1-4


SIGNAL 'I'
15
0
SIGNAL
2.7K
1K
10K
25pf
2.2K
1.6K
30
1K
OUTPUT
AMP
O FLIPFLOP
15
0
2.7K
1K
10K
30
25pf
2.2K
1.6K
1K
TO
CARRY
DRIVER
TO
M FLIPFLOP



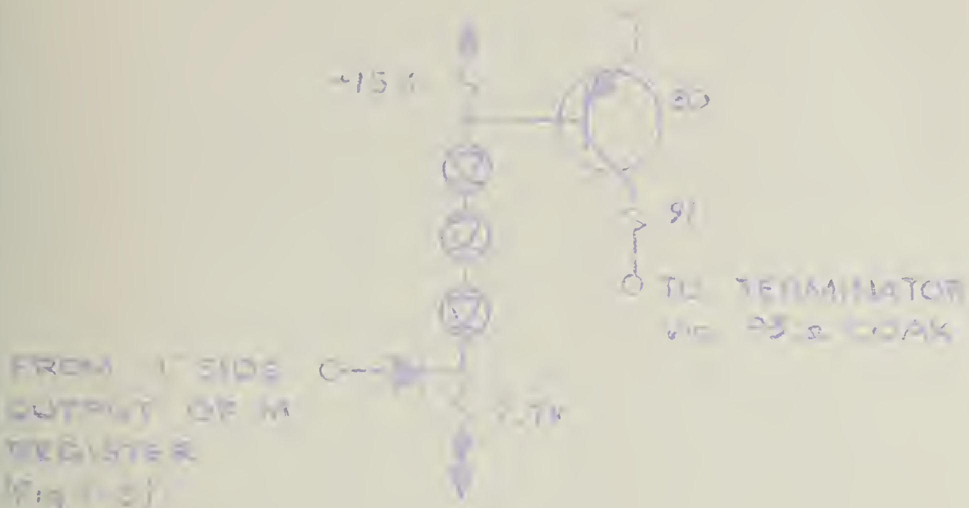
REGISTER FLIPFLOP 1-8
WITH BUBBLE AND DIRECT
INPUT GATES

Fig 1-6

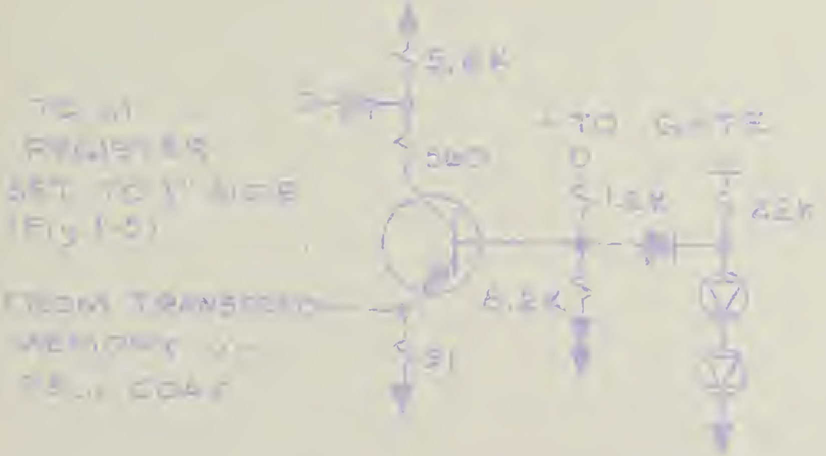


OUTPUT AND COMPLEMENT GAT
DIRECT TRANSFER OUTPUT DRI

Fig 1-7



CABLE DRIVER

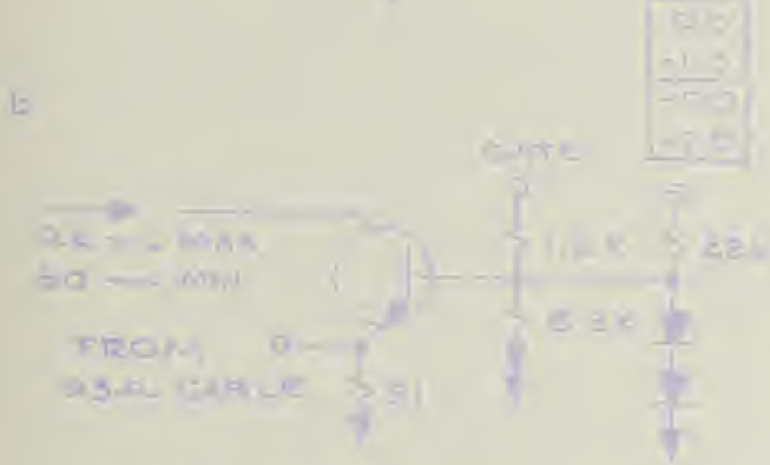


CABLE DRIVEN GATE

CABLE DRIVER AND CABLE DRIVEN GATE
FOR M FLIPFLOP

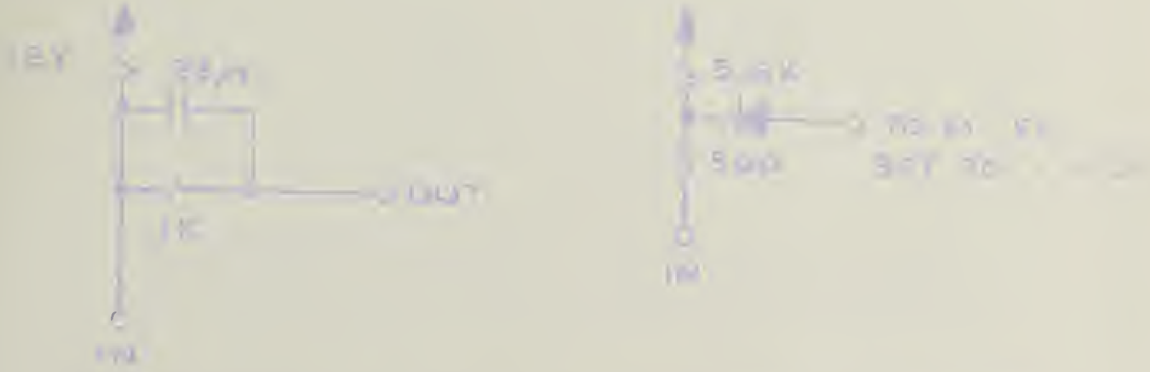
(Fig [illegible])

1-9b



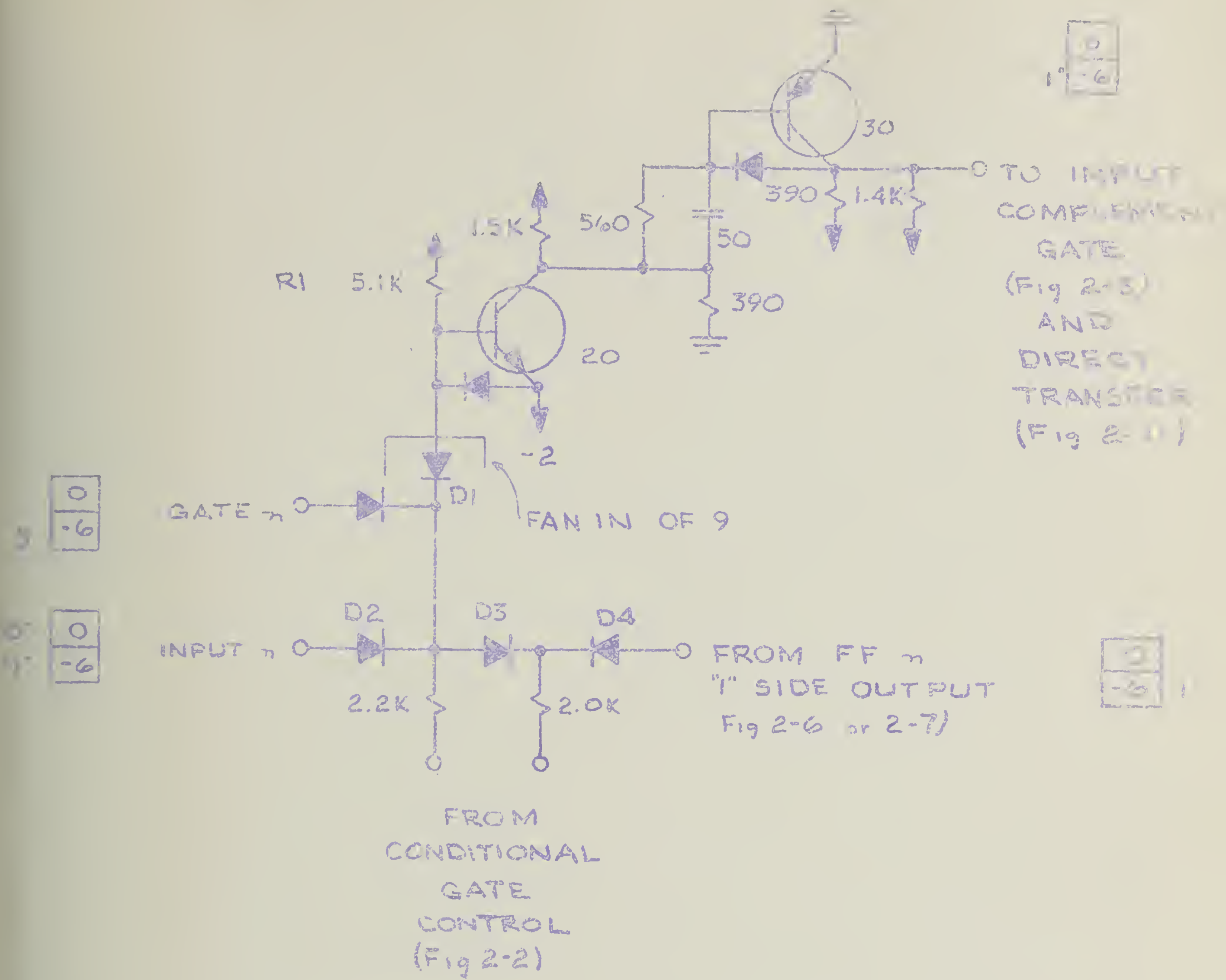
93Ω CABLE TERMINATORS

1-9c



TERMINATORS OPTIONAL LOAD CONFIGURATION

CABLE TERMINATORS



DIODES 1N955 TIS1

TRANS. PNP 2N965

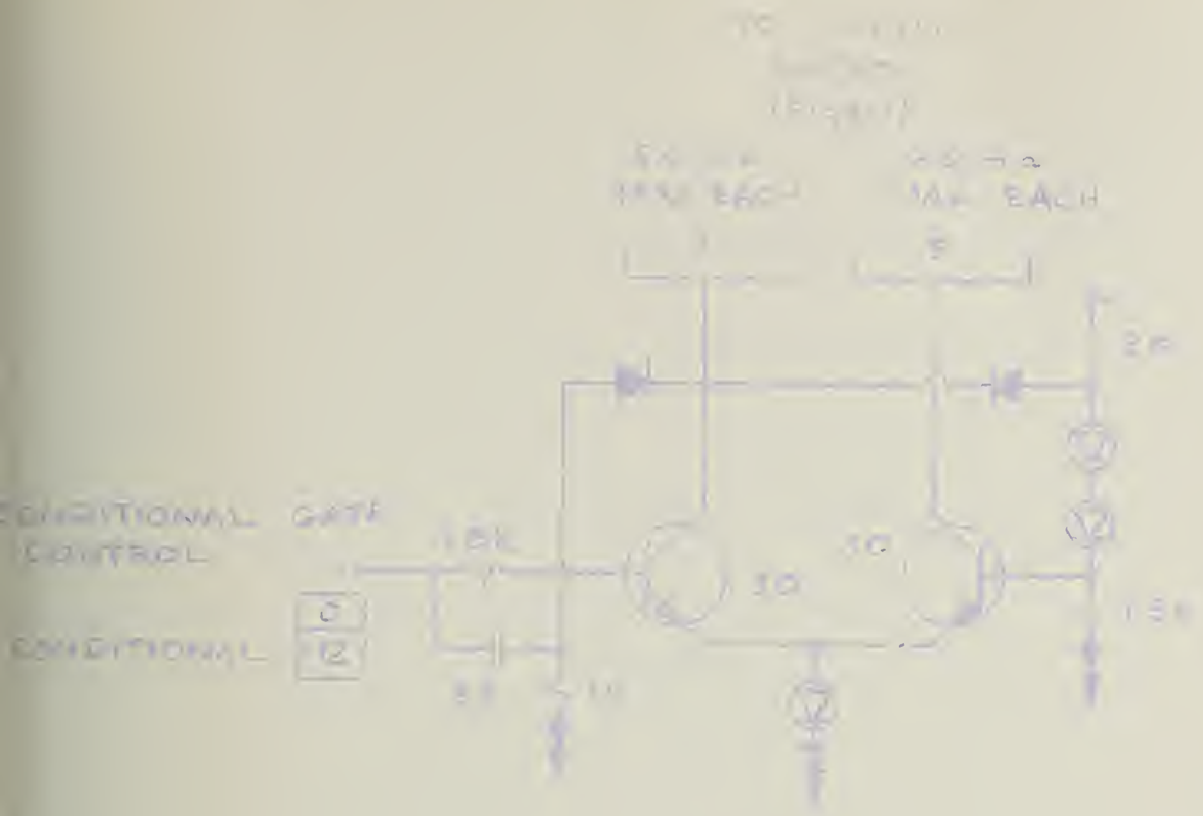
NPN 2N 797

NUMBER NEXT TO TRANSISTOR INDICATES MINIMUM β FOR DESIGN

☐ GIVES NOMINAL SIGNAL SWING

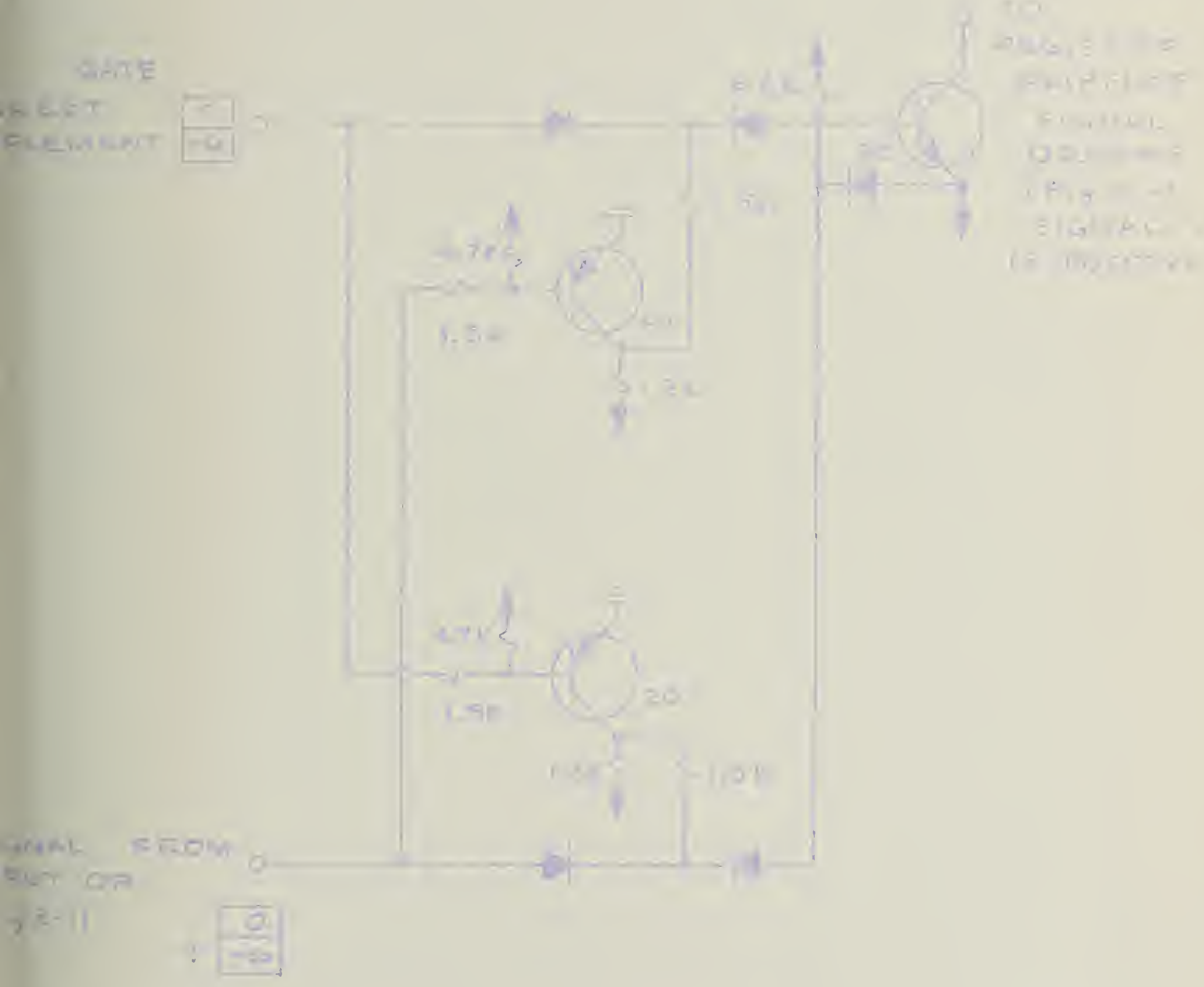
INPUT OR GATE

Fig 2-1



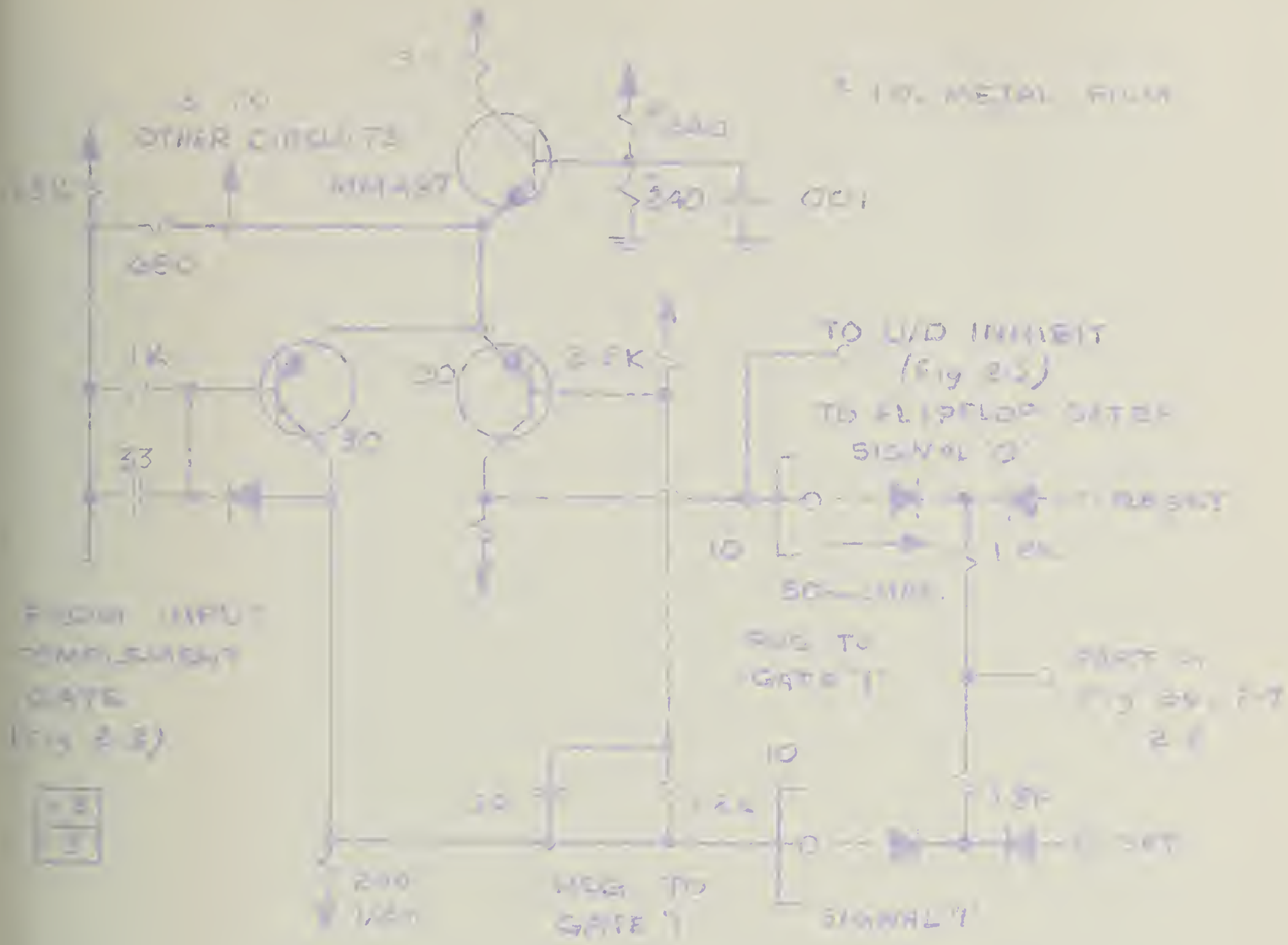
CONDITIONAL GATE CONTROL

FIG 8.2



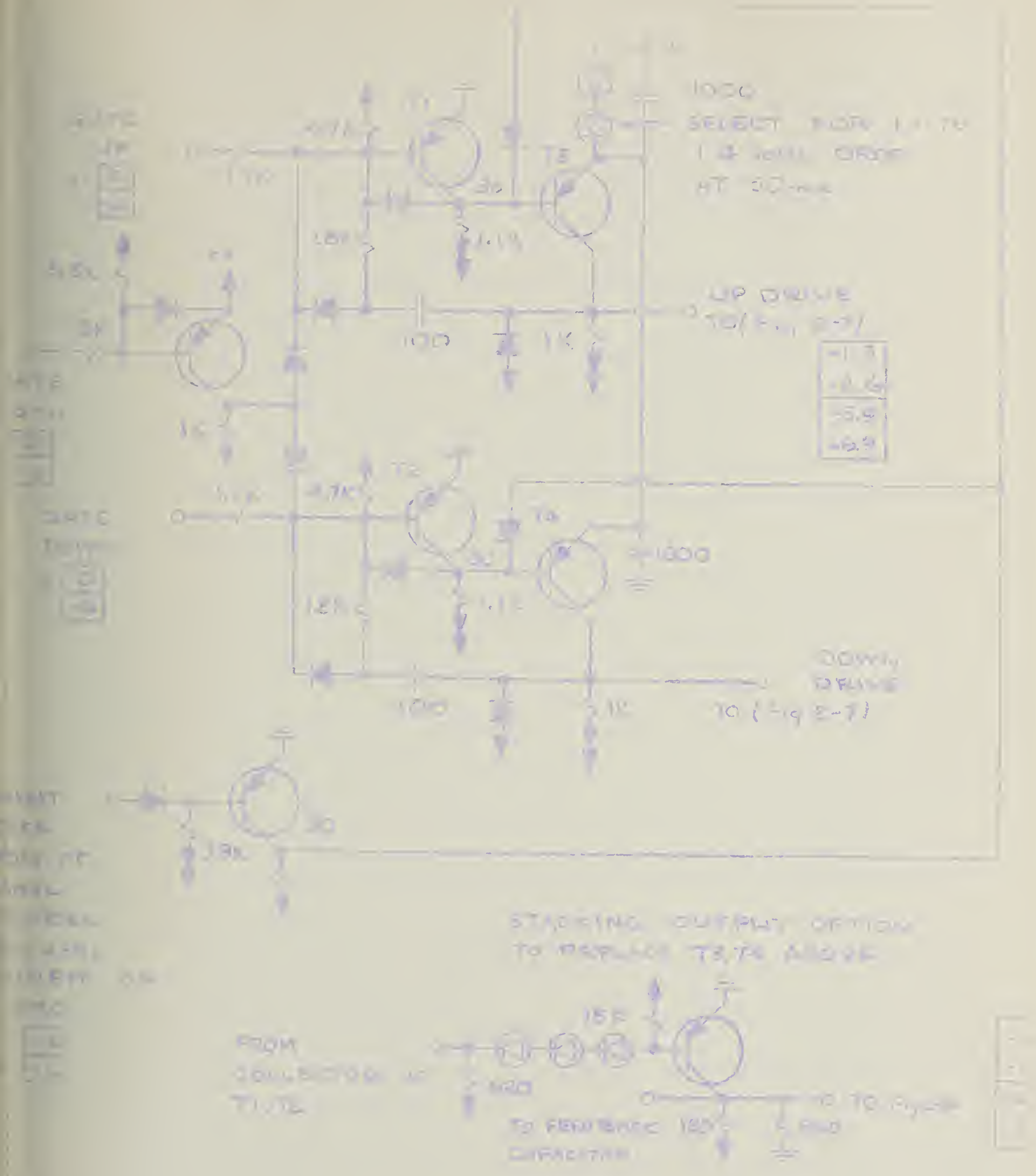
INPUT COMPLEMENT GATE

Fig. 2-3



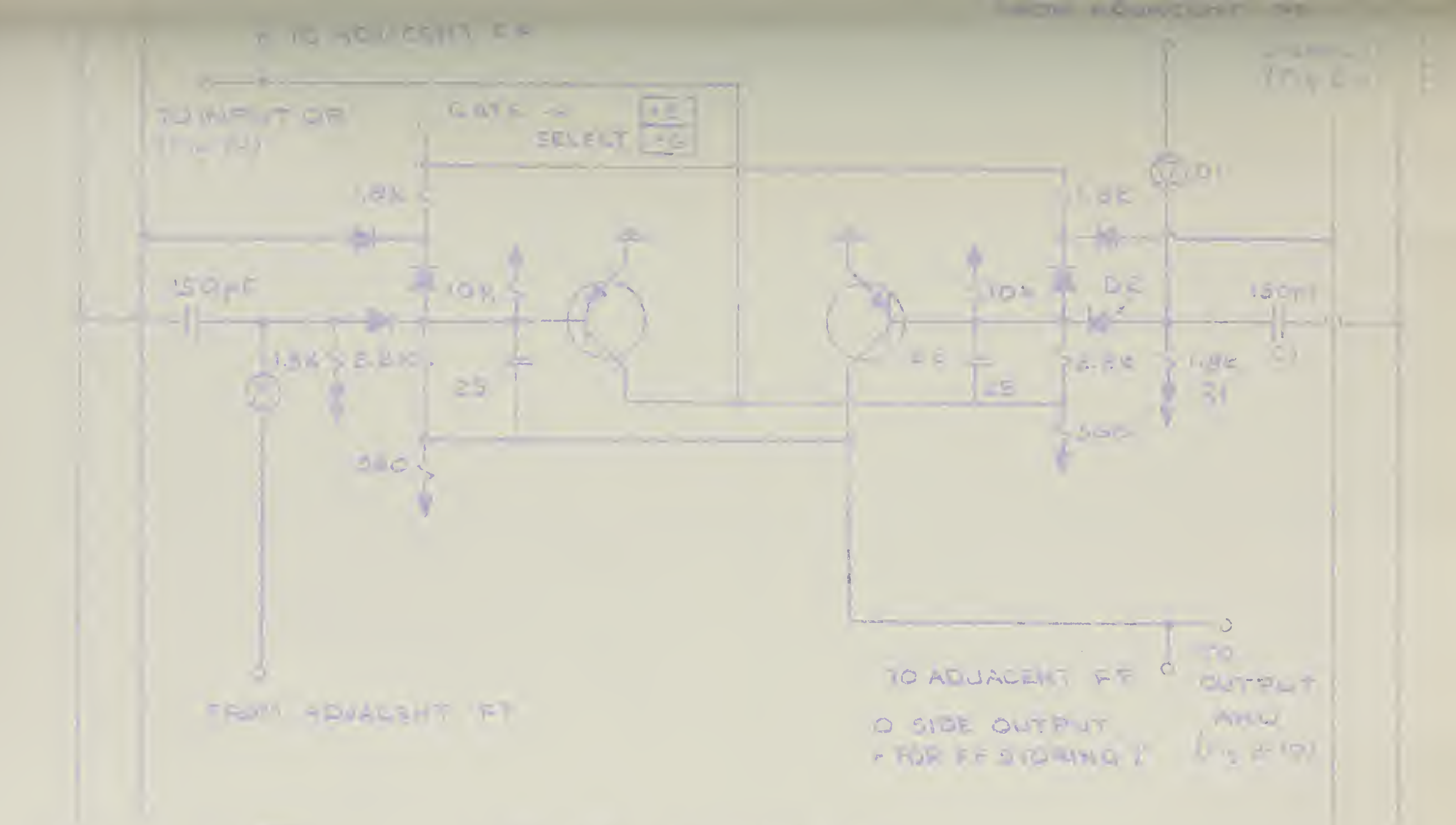
BOOSTING FLIPFLOP SIGNAL DRIVER

Fig 2-[illegible]



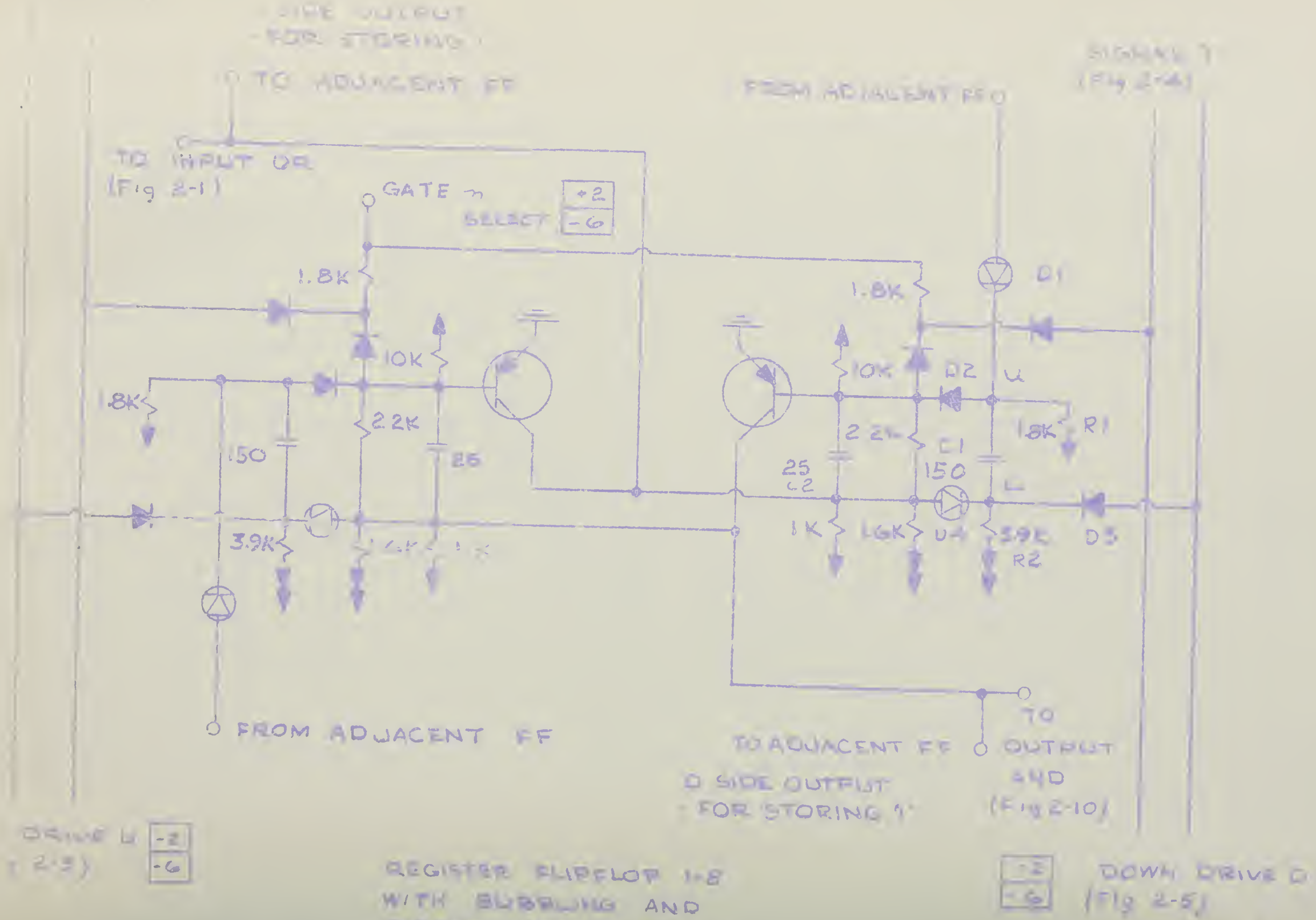
UP AND DOWN DRIVERS

Fig 2-6



REGISTER FLIPFLOP 1-2
WITH STACKING AND
DIRECT INPUT GATES

Fig 2-6



REGISTER FLIPFLOP 1-8
WITH BUBBLING AND
DIRECT INPUT GATES

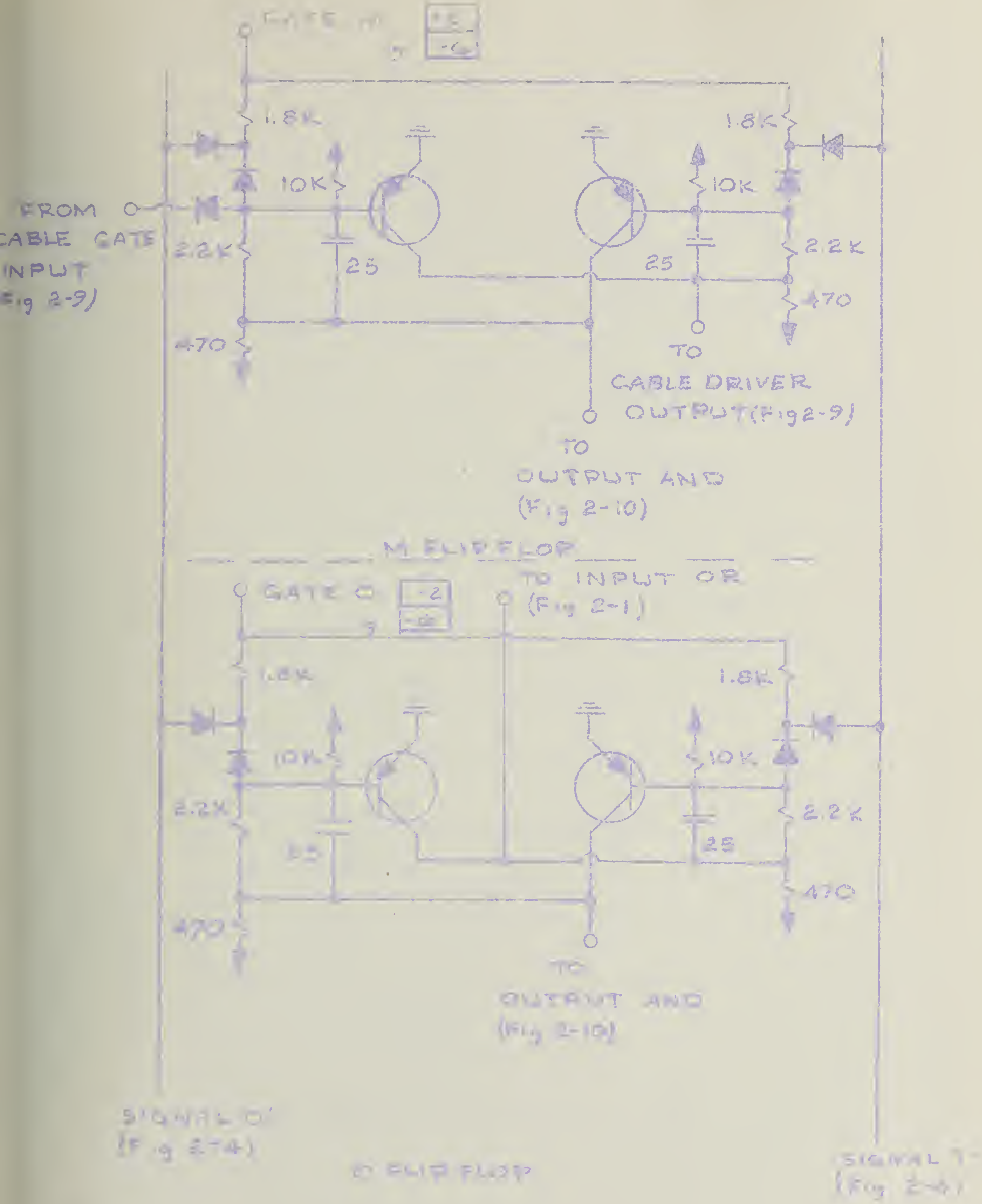
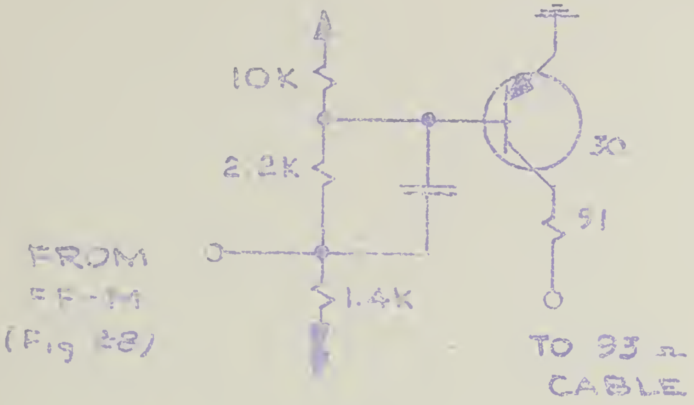
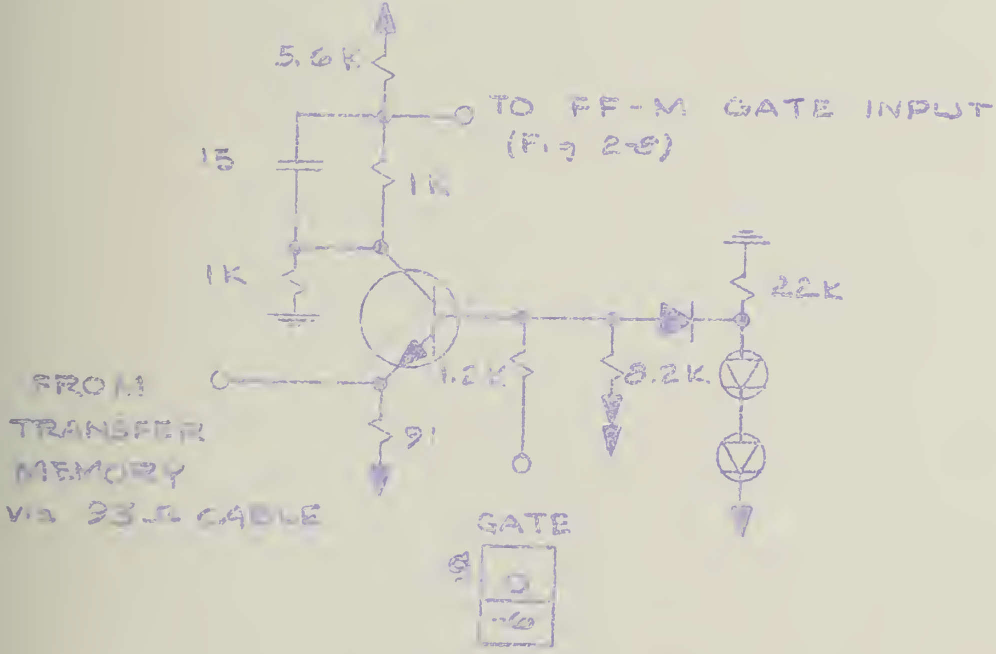

GATE M
+5
-6
5
1.8K
1.8K
10K
10K
FROM CABLE GATE INPUT (Fig 2-9)
2.2K
2.2K
25
25
470
470
TO CABLE DRIVER OUTPUT (Fig 2-9)
TO OUTPUT AND (Fig 2-10)
M FLIP FLOP
GATE D
-2
-6
5
TO INPUT OR (Fig 2-1)
1.8K
1.8K
10K
10K
2.2K
2.2K
25
25
470
470
TO OUTPUT AND (Fig 2-10)
SIGNAL 0 (Fig 2-4)
D FLIP FLOP
SIGNAL 1 (Fig 2-4)

Fig 2-8



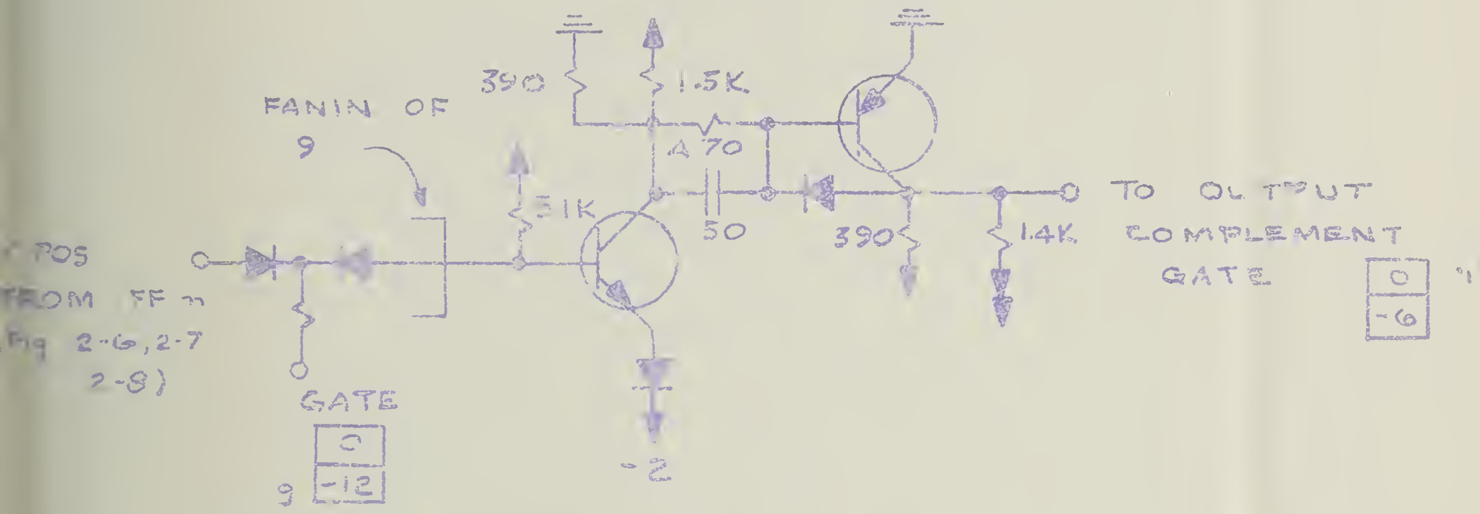
OUTPUT CABLE DRIVER



TERMINATED CABLE GATE

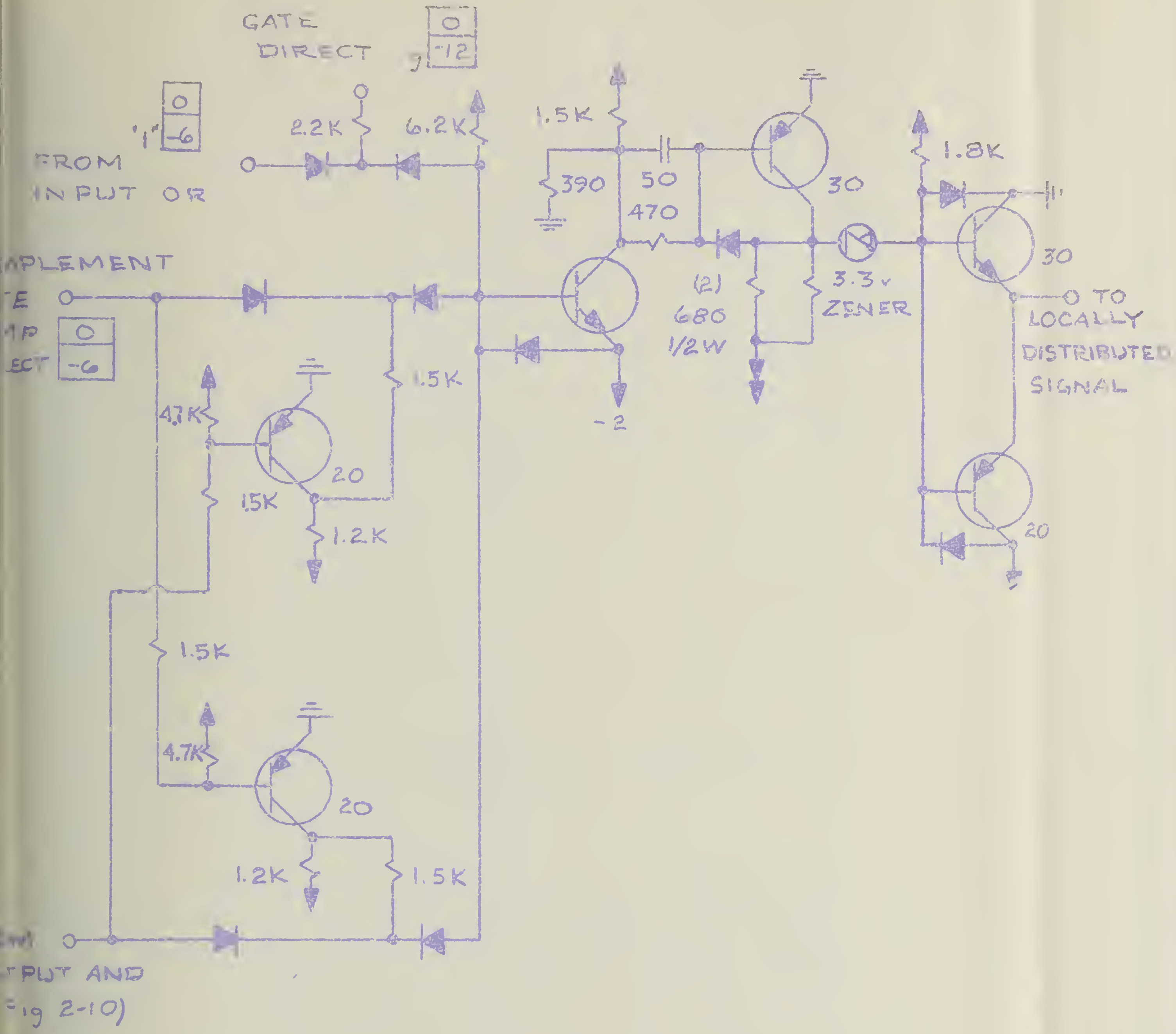
M-FF CONNECTIONS

Fig 2-9



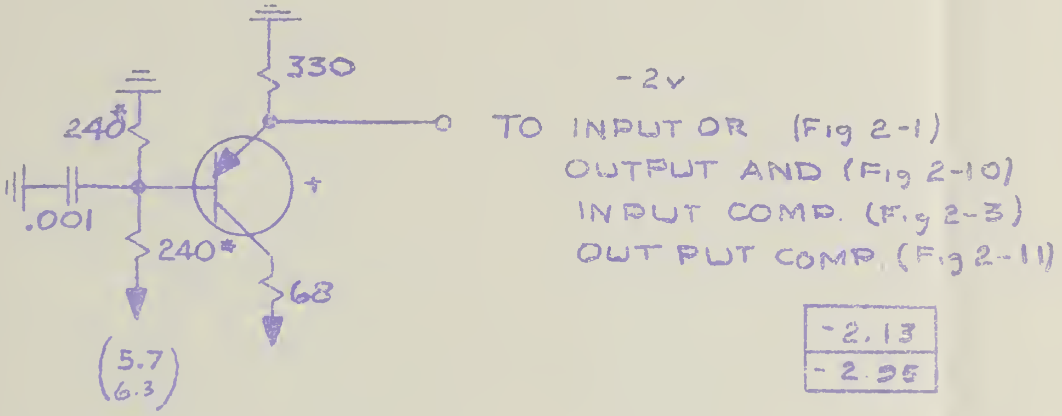
OUTPUT AND GATE

Fig 2-10



OUTPUT COMPLEMENT GATE, OUTPUT OR, AND OUTPUT DRIVERS

Fig 2-11



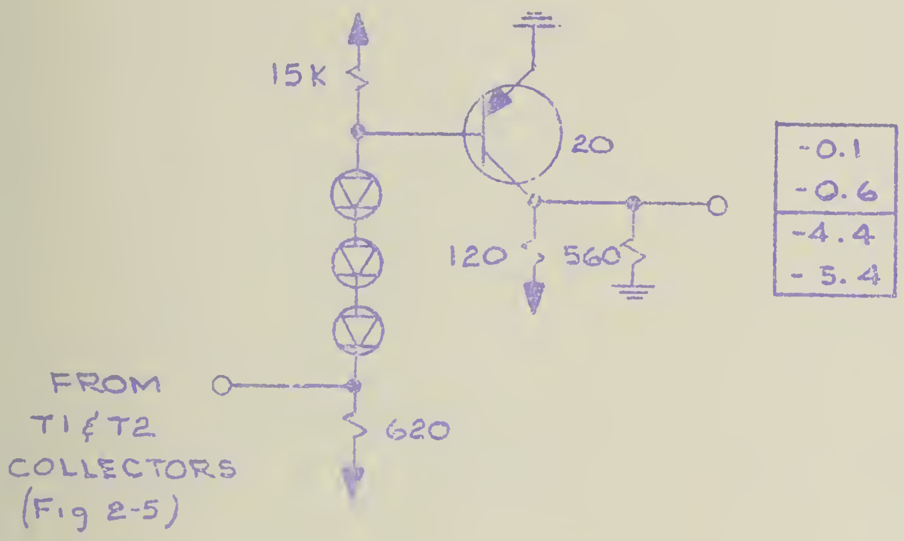
TO INPUT OR (Fig 2-1)
OUTPUT AND (Fig 2-10)
INPUT COMP. (Fig 2-3)
OUTPUT COMP. (Fig 2-11)

* PRECISION 1% METAL FILM
DESIGN 5%

+ SELECTED FOR HIGH β, LOW Veb fwd AT 40 ma
DESIGN β = 30
Veb = .3 TO .6 AT 40 ma

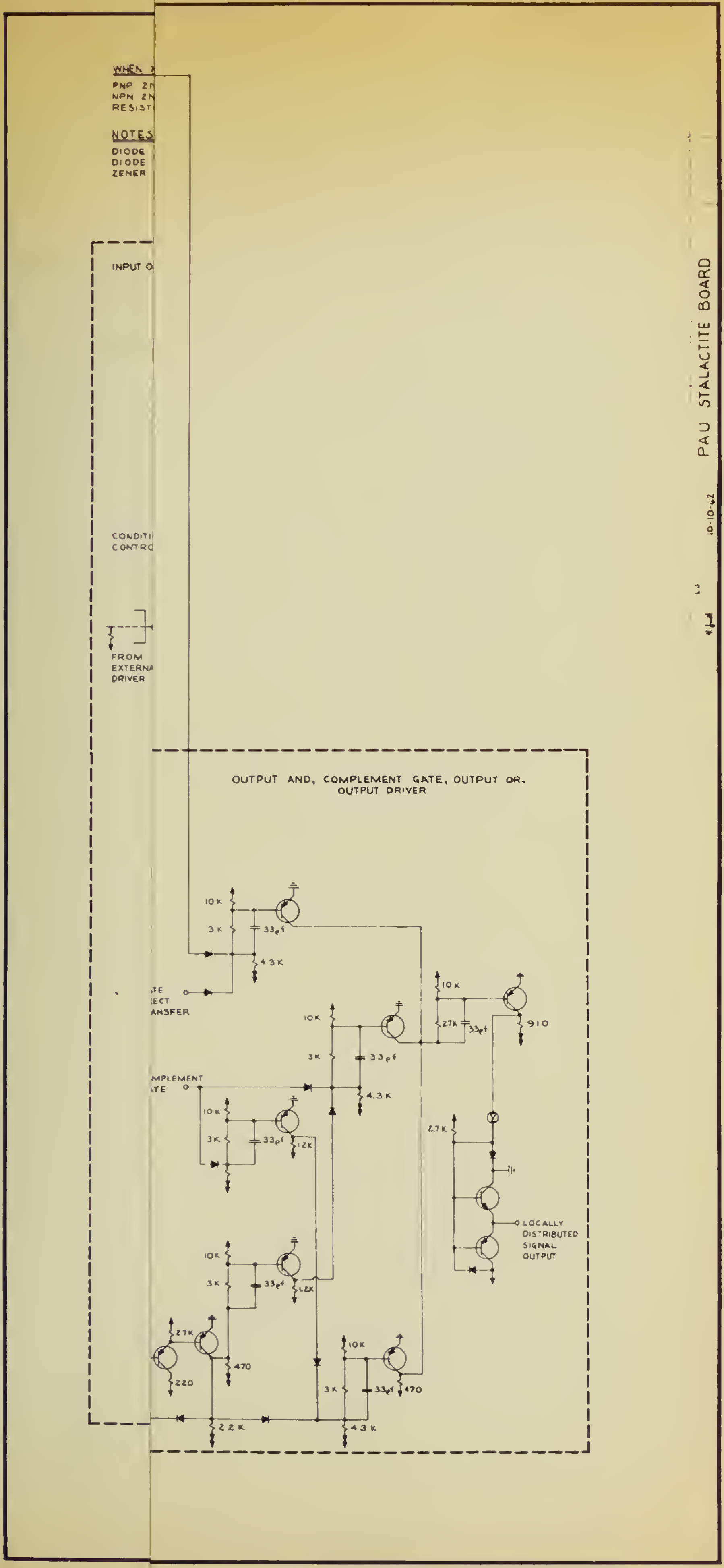
-2 VOLT SUPPLY

Fig 2-12



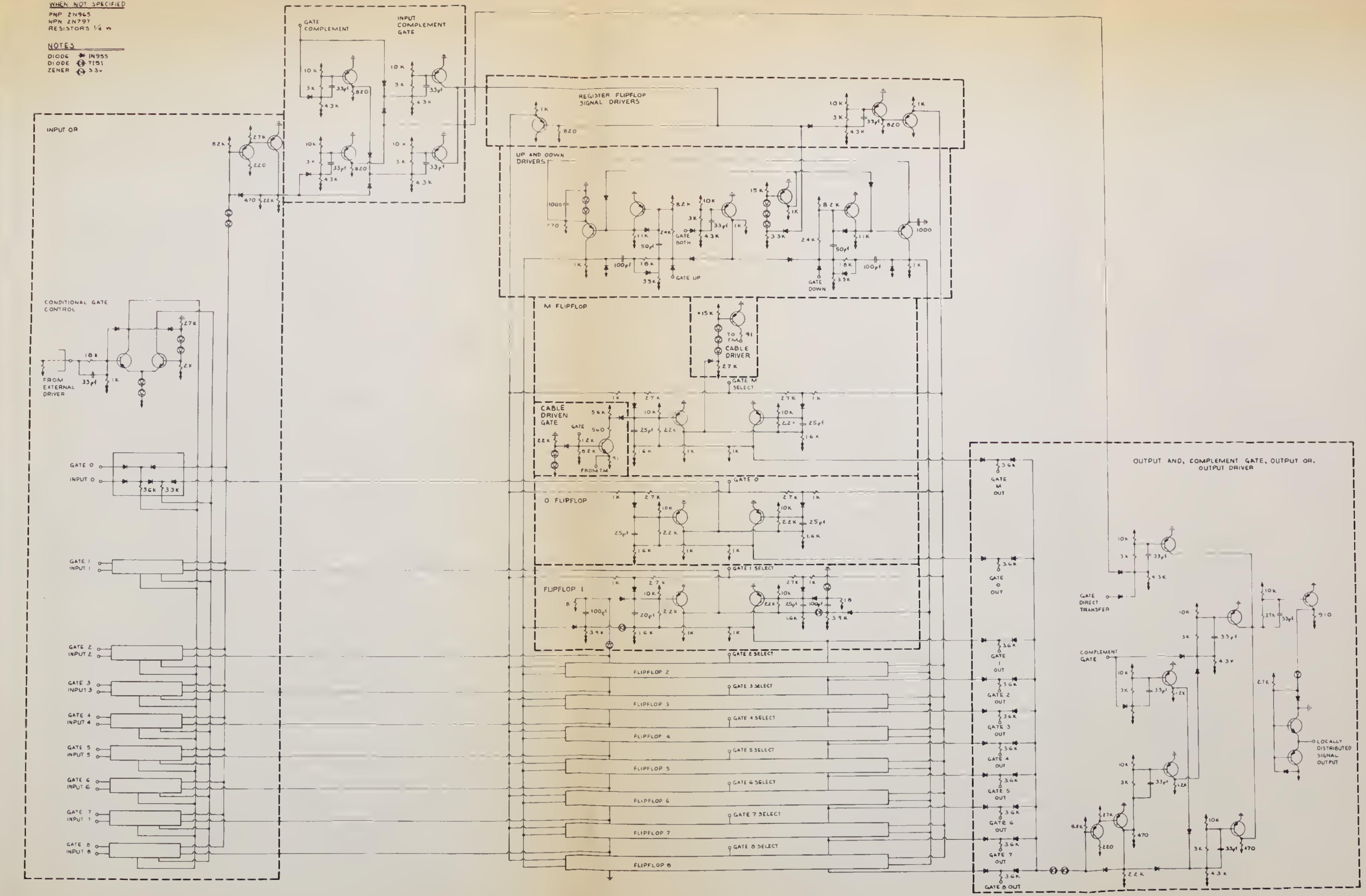
OUTPUT CIRCUIT FOR
STACKING LOGIC UP/DOWN DRIVER

Fig 2-13



PAU STALACTITE BOARD

10-10-62



PAU STALACTITE BOARD

10 10 62

ERRATA TO REPORT NO. 127

In Report No. 127, the fold-out schematic of the entire stalactite contains several errors in the gating circuits between the flipflops of the Stacking/Bubbling register. The schematic, as shown, indicates that the "1" side of flipflop N gates down to the base of the "1" side of flipflop (N + 1). It also shows the "0" side of flipflop N as gating up to the "0" side of flipflop (N - 1).

Actually, however, as indicated in the correction, each flipflop's collector gates to the "opposite" base of the appropriate flipflop. Changes are indicated by a dashed (——·——·——) line.